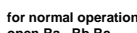
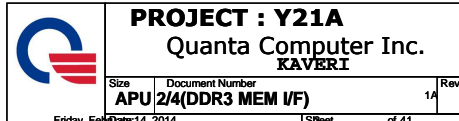


APU\_TRST# R234 1Kf 4 4 APU  
APU\_DBREQ# R212 1Kf 4 4 APU  
4/19 For Comal. 4 APU

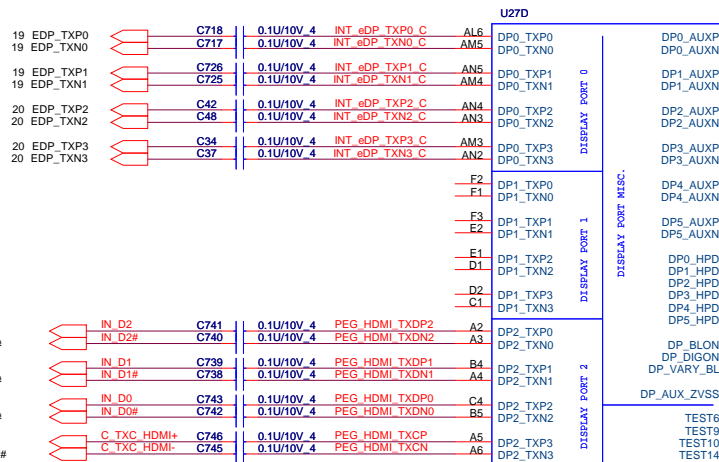


4,6,8,9,10,11,12,19,20,21,22,23,24,25,26,27,28,29,30,38 +1.35V  
+3V  
4,22,27,29,34 +1.5V  
3,4,5,11,12,33,38 +1.35VSUS  
4.5 +1.05V VDD





DP0 output to  
eDP to LVDS converter



4/19 HDMI change to DP2 for Comal.

DP2 output to  
HDMI connector

note --HDMI P&N can not swap

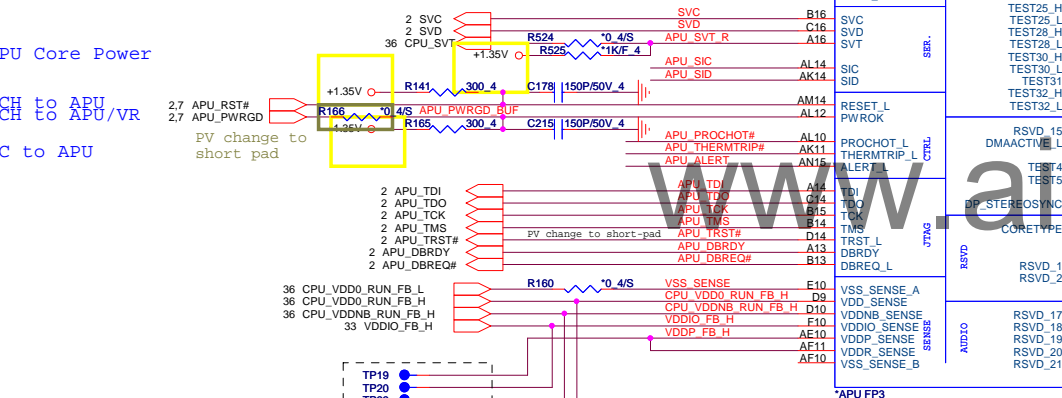
Note: CLK APU HCLKP/N is 100MHZ SSC

Note: CLK\_DP\_NSSCP/N is 100MHZ non-SSC

APU Core Power

FCH to APU, ...

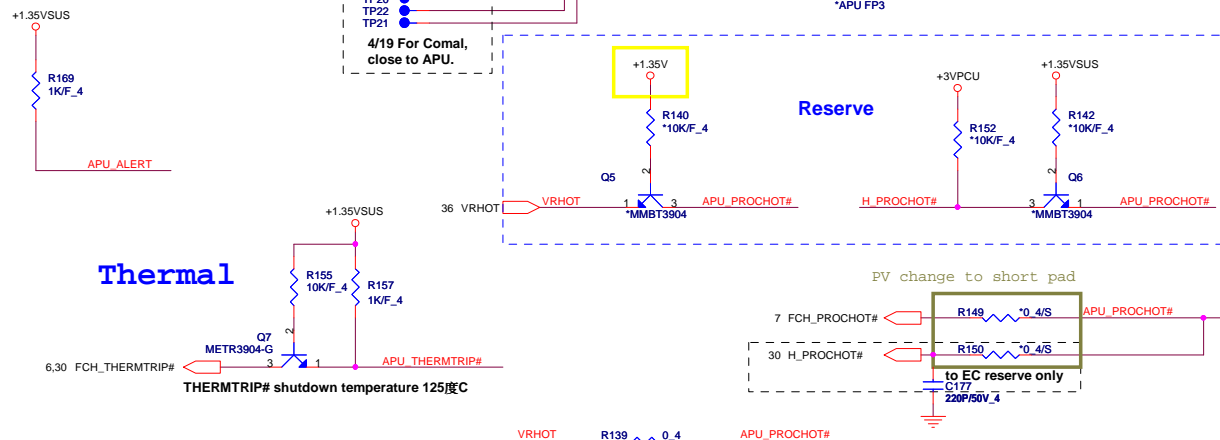
EC to APU



4/19 For Comal,  
close to APU.

## Reserve

## Thermal

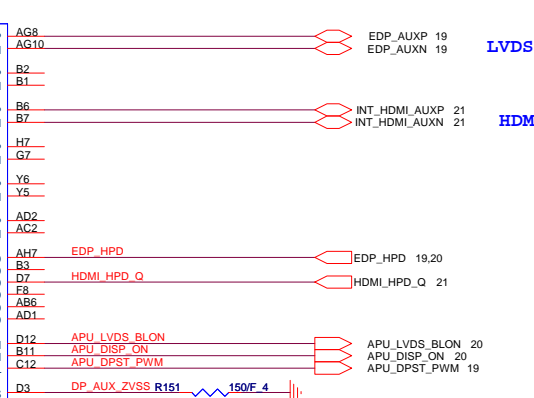


**THERMTRIP# shutdown temperature 125°C**

VRHOT R139 0.4 APU\_PROCHOT#

## LVDS

## HDMI



DISPLAY PORT MISC.

TEST

[illegible]

IO	RSVD
----	------

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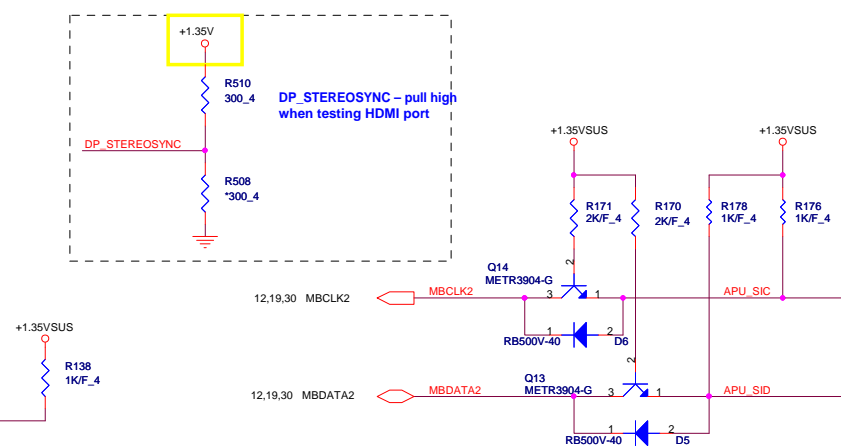
—

$$\text{---R'}$$

---

**DMAACTIVE\_L** controls entry and exit from the sleep and power states

DP\_STEREO\_SYNC – pull high when testing HDMI port



2,6,8,9,10,11,12,19,20,21,22,23,24,25,26,27,28,29,30,38 +1.35V  
+3V  
2.5 +1.05V\_VDDP  
2,22,27,29,34 +1.5V  
2,3,5,11,12,33,38 +1.35VSUS

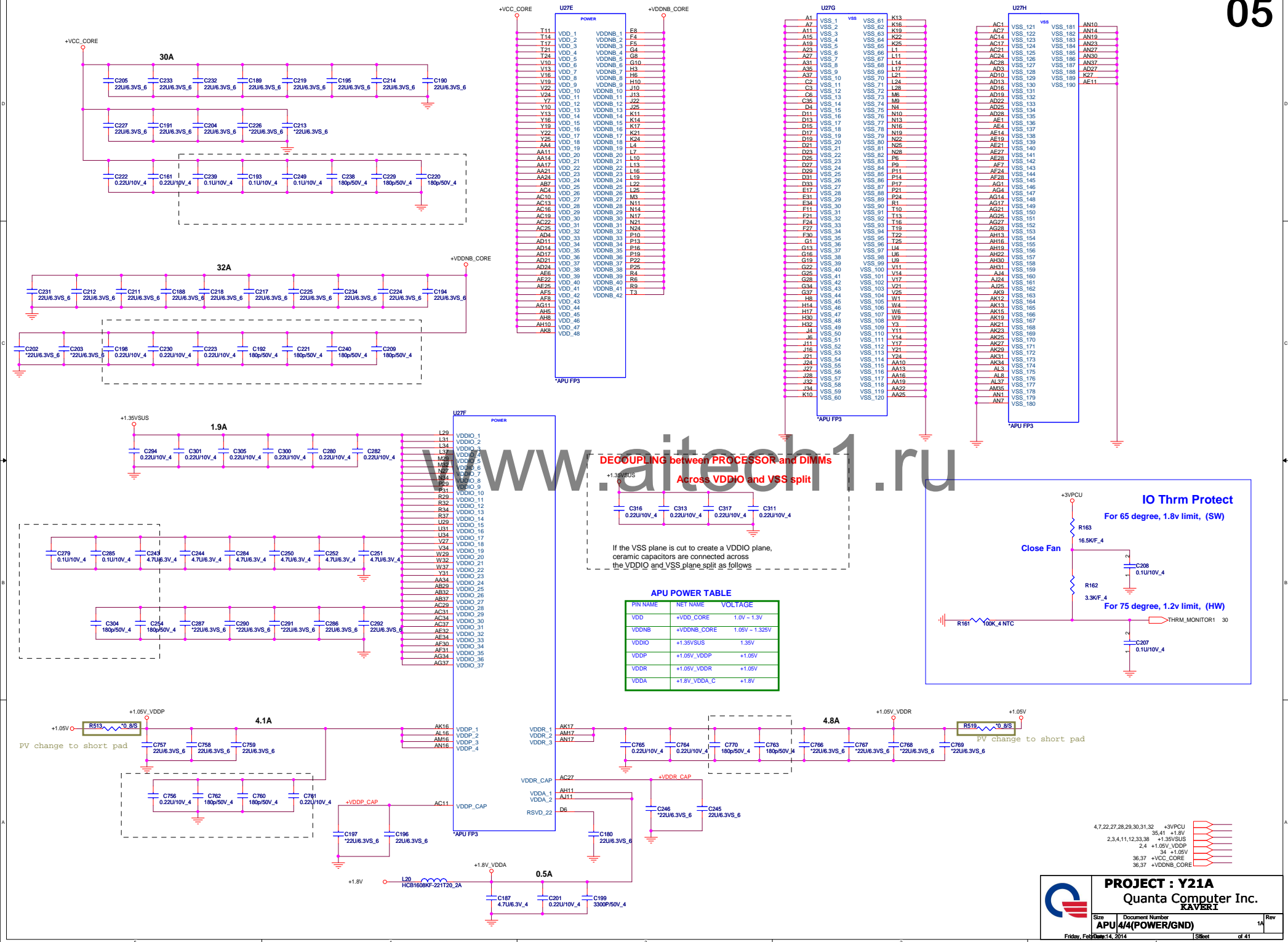


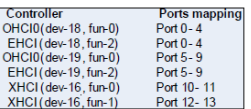
**PROJECT : Y21A**  
Quanta Computer Inc.

Size	Document Number	Rev
APU 3/4(Display/Misc/HPT)		1A

Friday, February 14, 2014 Sheet 1 of 41





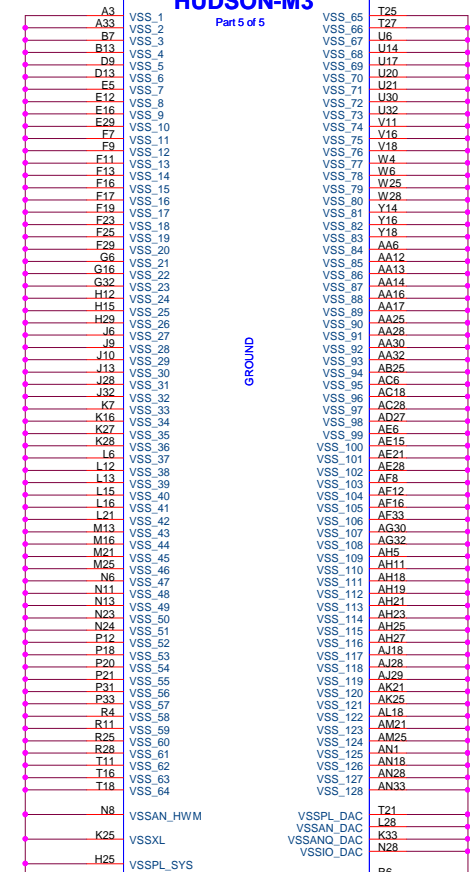


SCL3 of a TSI-capable APU's thermal bus, Pulled up to APU\_VDDIO. Resistor value verified in the relevant APU design guide.



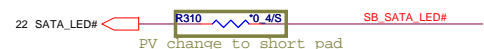
## HUDSON-M3

Part 5 of 5



SATA HDD

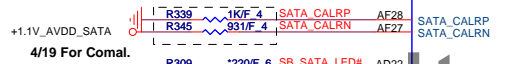
SATA ODD



PV change to short pad



PLACE SATA\_CAL RES VERY  
CLOSE TO BALL OF  
HUDSON-M2/M3



Integrated Clock Mode:  
Leave unconnected.

GPIO52 internal pull Hi 8.2K to +3V  
GPIO53 internal pull Hi 8.2K to +3V  
GPIO54 internal pull Hi 8.2K to +3V  
GPIO55 internal pull Hi 8.2K to +3V  
GPIO57 internal pull Hi 8.2K to +3V  
GPIO58 internal pull Hi 8.2K to +3V

BT\_COMBO OFF# AH16  
BT\_COMBO EN# AH16  
ODD\_PWR AK15  
ACC\_LED# TP87

TEMPINO K6  
TEMPIN1 K5  
TEMPIN2 K3  
TEMPIN3 M6

R391 10K/F 4  
R390 10K/F 4  
R597 10K/F 4  
R389 10K/F 4

Hudson-M3-A14  
TEMP (0 - 3)  
Temp Monitor Not Implemented  
10-K 5% pull-up to +3VS5  
or 10-K 5% pull-down

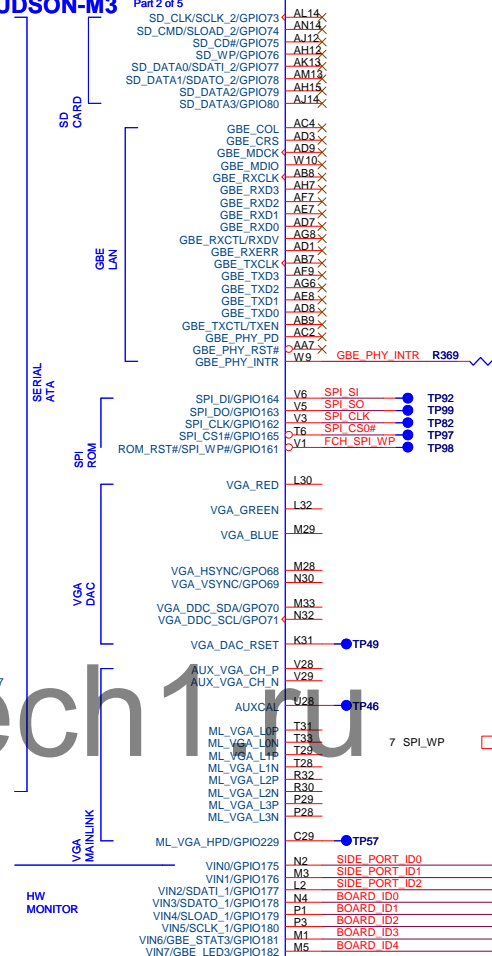
Board ID [4:3]	Definition
00	Pavilion
01	Envy
01	Pavilion Special Edition
11	TBD

Board ID 0	Definition
0	UMA
1	SG

Board ID [2:1]	Definition
00	14"
01	15"
10	17"

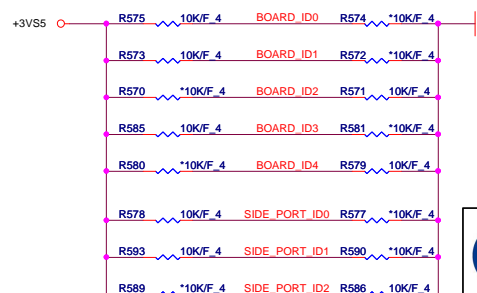
## HUDSON-M3

Part 2 of 5

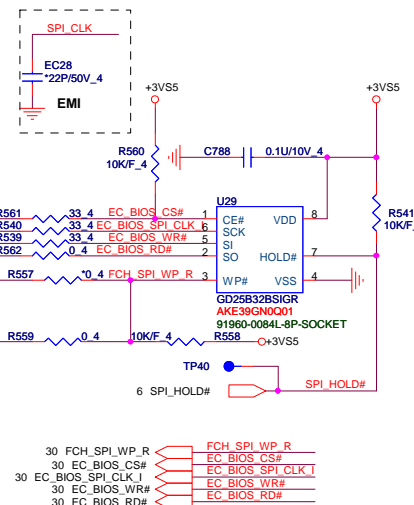


HW MONITOR

VIN (0 - 7)  
Voltage Monitor Not Implemented  
10-K 5% pull-up to +3VS5  
or 10-K 5% pull-down



Vender	Size	P/N
Giga	4M	AKE39GN0Q01
EON	4M	AKE39ZN0Q03
WND	4M	AKE39FN0N01
Socket		DFHS08FS023



30 FCH\_SPI\_WP\_R  $\rightarrow$  FCH\_SPI\_WP\_R  
30 EC\_BIOS\_CS#  $\rightarrow$  EC\_BIOS\_CS#  
30 EC\_BIOS\_SPI\_CLK\_I  $\rightarrow$  EC\_BIOS\_SPI\_CLK\_I  
30 EC\_BIOS\_WR#  $\rightarrow$  EC\_BIOS\_WR#  
30 EC\_BIOS\_RD#  $\rightarrow$  EC\_BIOS\_RD#

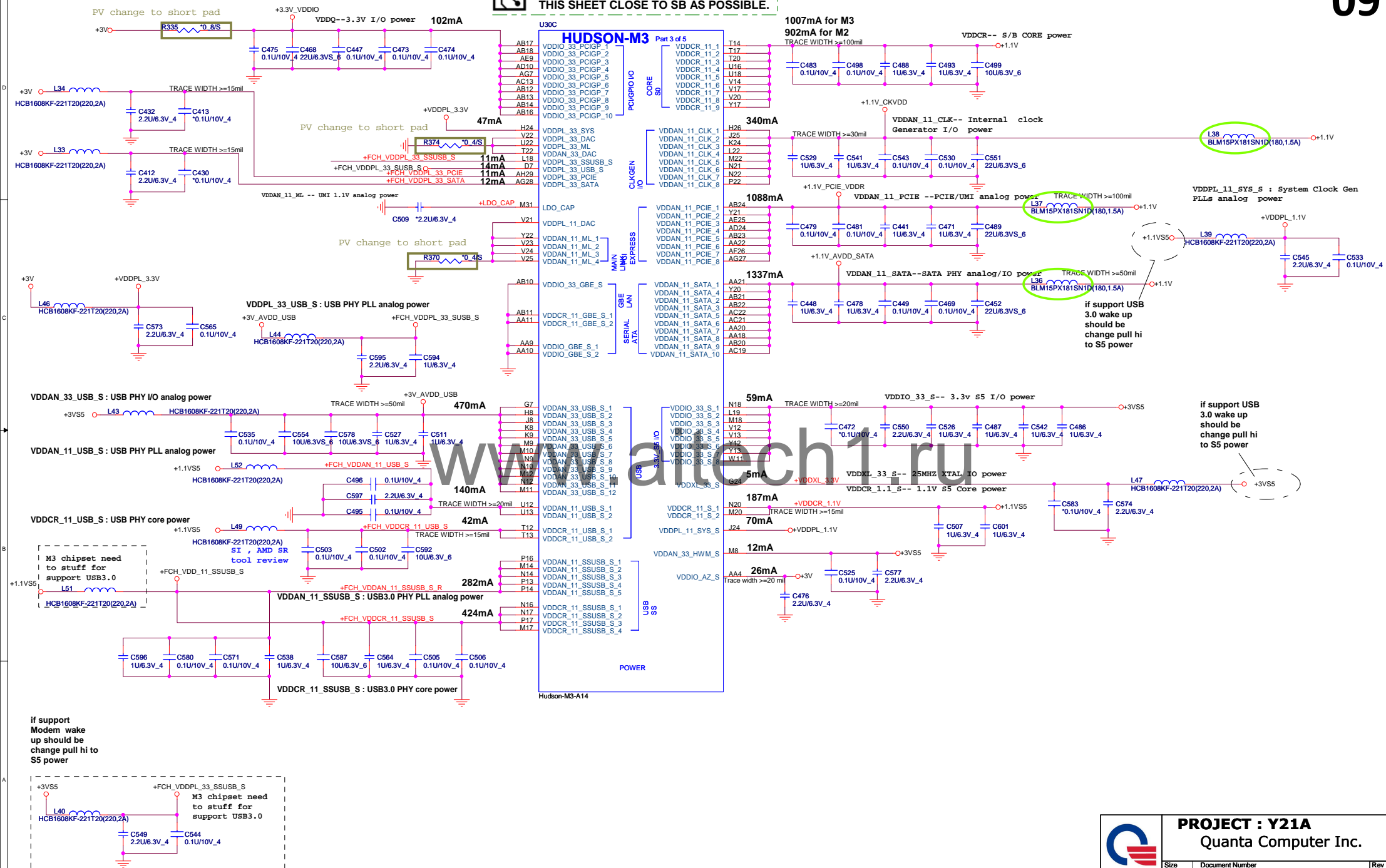


PROJECT : Y21A  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 SATA/HWM/SPI	1A
Date: Monday, February 17, 2014	Sheet 8 of 41	



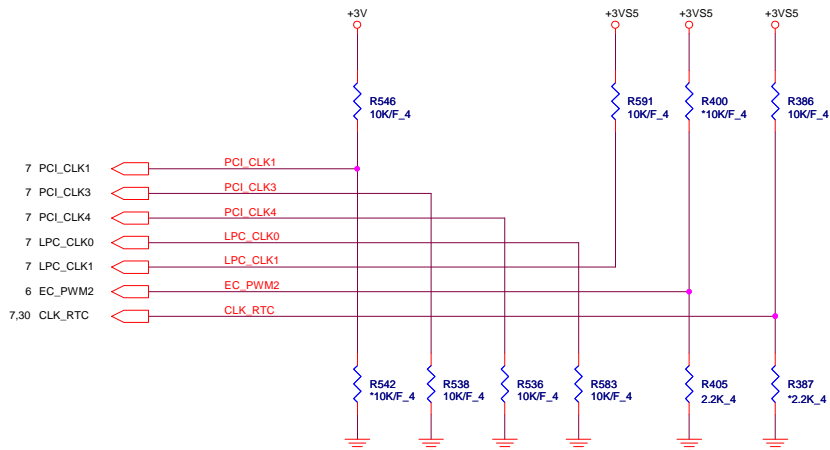
**PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.**





STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2  DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED  DEFAULT	LPC ROM	S5 PLUS MODE ENABLED  DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	SPI ROM DEFAULT	S5 PLUS MODE DISABLED

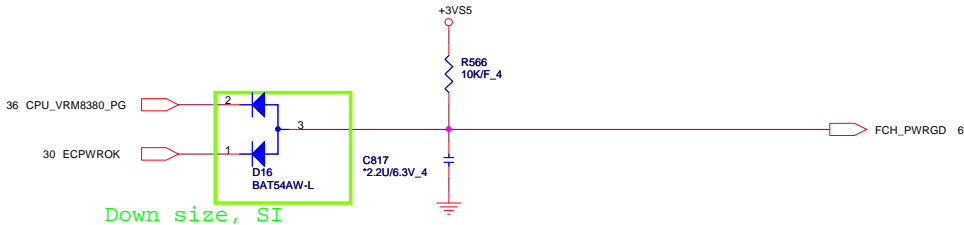
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI\_AD[27:23]

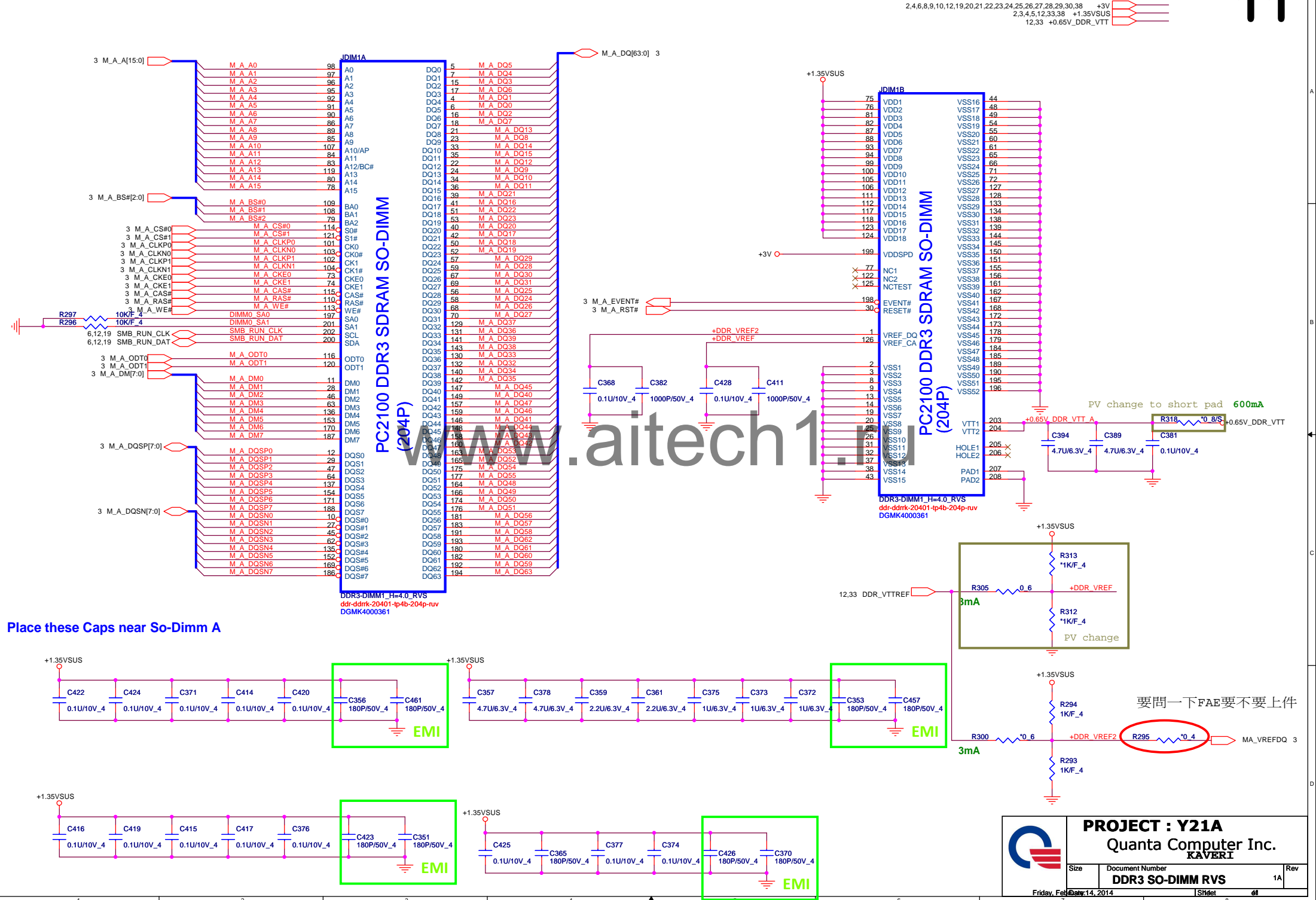


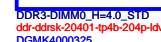
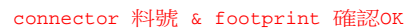
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL  DEFAULT	DISABLE ILA AUTORUN  DEFAULT	USE FC PLL  DEFAULT	USE DEFAULT PCIE STRAPS  DEFAULT	DISABLE PCI MEM BOOT  DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH\_PWRGD

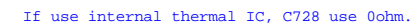
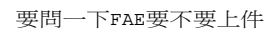



Down size, SI

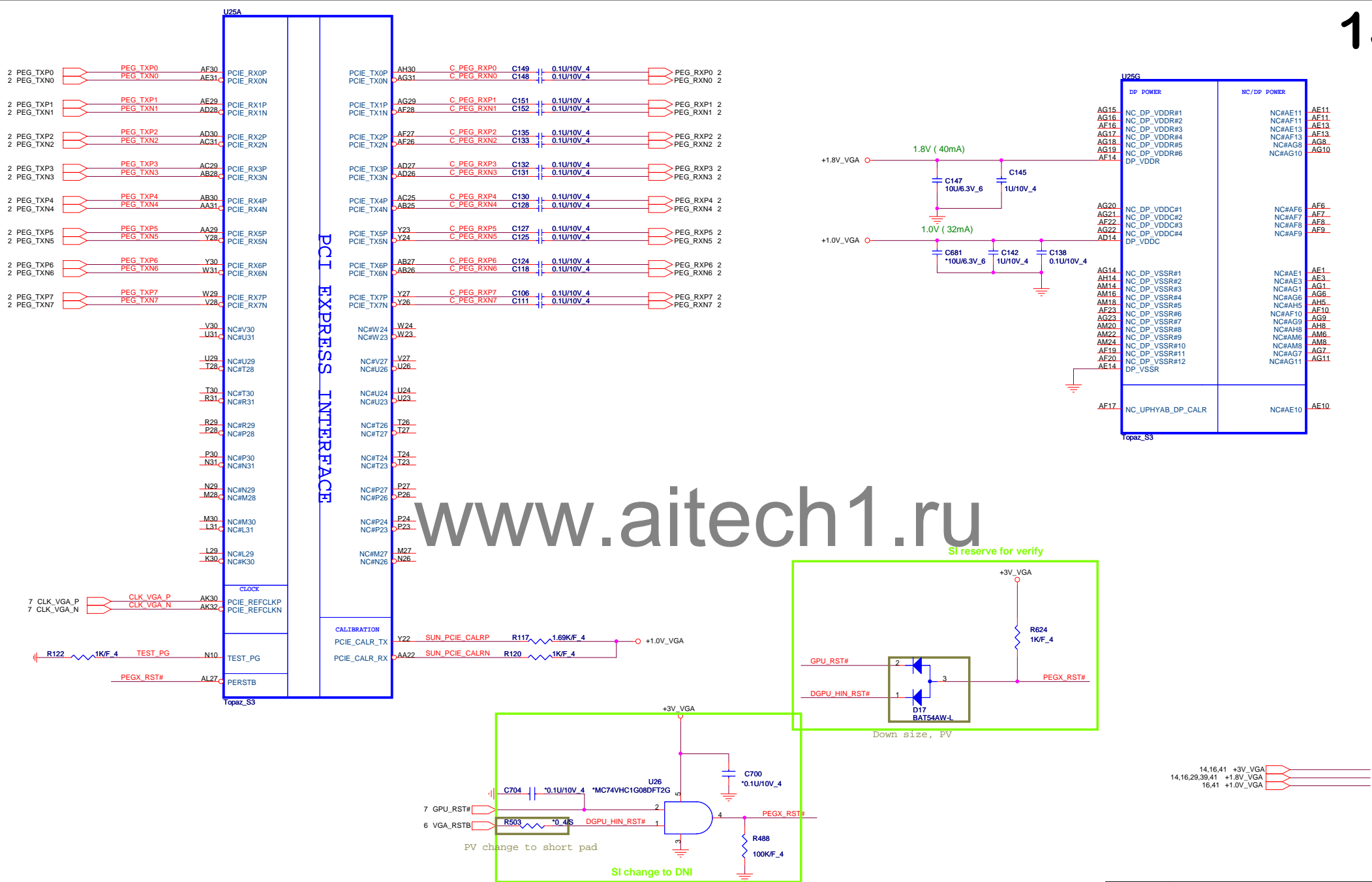


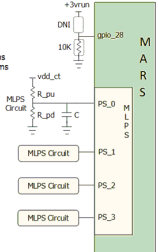


DDR3-DIMM0\_H=4.0\_STD  
ddr-ddrsk-20401-tp4b-204p-ldev  
DGMK4000325



	<b>PROJECT : Y21A</b> <b>Quanta Computer Inc.</b> <b>KAVERI</b>		
	Size	Document Number	Rev
		<b>DDR3 SO-DIMM STD</b>	<b>1A</b>
Friday, February 14, 2014	Sheet	of 41	



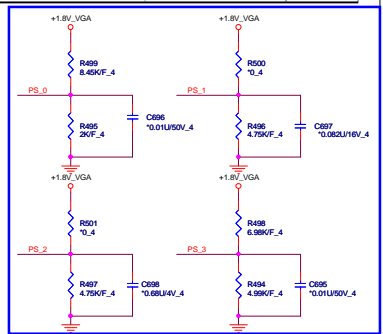


### MLPS Implementation

- Connect GPIO\_28 to 10K pulldown to enable MLPS
- If any of PS\_0/1/2/3 is not used, leave "no connect"
- R<sub>pu</sub>, R<sub>pd</sub> and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohm
- Total DC resistance of trace between C and ground should be less than 2 ohm
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

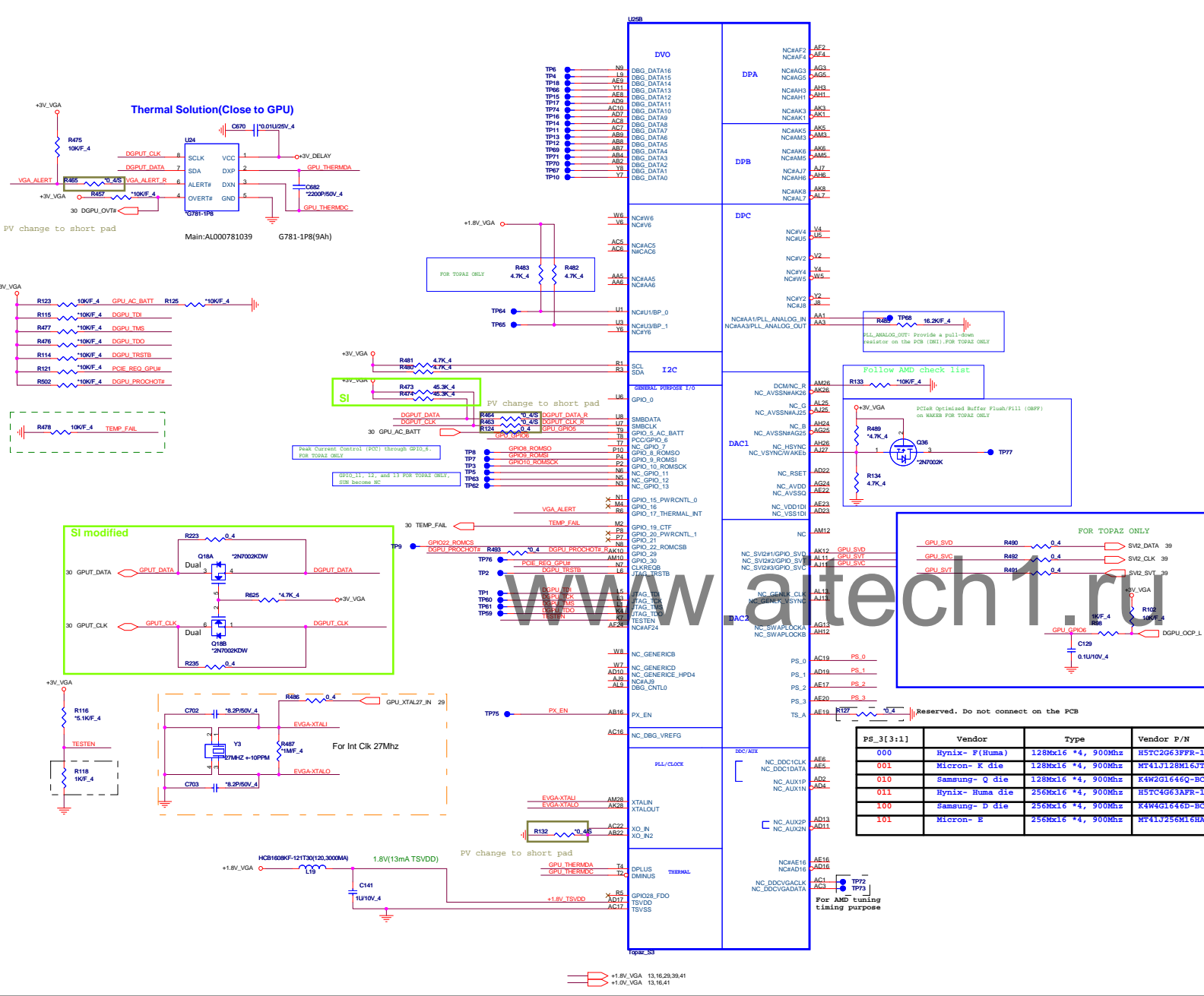
Capacitor Lookup Table		Resistor Divider Lookup Table		
C (nF)	Bits[5,4]	R <sub>pu</sub> (Ohm)	R <sub>pd</sub> (Ohm)	Bits(3,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[11]	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_0[12]	ROM_CONFIG[1]	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 29).	
PS_0[13]	ROM_CONFIG[2]	Reserved for internal use only.	
PS_0[14]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[15]	N/A	Reserved.	1
PS_1[11]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 - PCIe GEN3 is supported. 0 - PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[12]	STRAP_BIF_CLK_RM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 0 - The CLKREQ# power management capability is disabled. 1 - The CLKREQ# power management capability is enabled.	0
PS_1[13]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[14]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode. 0 - The transmitter half-swing is enabled. 1 - The transmitter full-swing is enabled.	1
PS_1[15]	STRAP_TX_DEEMP_PH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 - Tx deemphasis disabled. 1 - Tx deemphasis enabled.	Design dependent, see the description.
PS_2[11]	N/A	Reserved.	0
PS_2[12]	N/A	Reserved.	0
PS_2[13]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 - Disable the external BIOS ROM device. 1 - Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[14]	N/A	Reserved.	1
PS_2[15]	N/A	Reserved.	1
PS_3[11]	BOARD_CONFIG[0]	Board configuration related strapings, such as for memory ID	Design dependent, see the description.
PS_3[12]	BOARD_CONFIG[1]		
PS_3[13]	BOARD_CONFIG[2]		
PS_3[14]	N/A	Reserved.	1
PS_3[15]	N/A	Reserved.	1

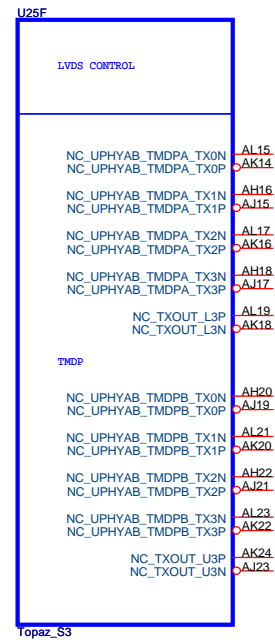
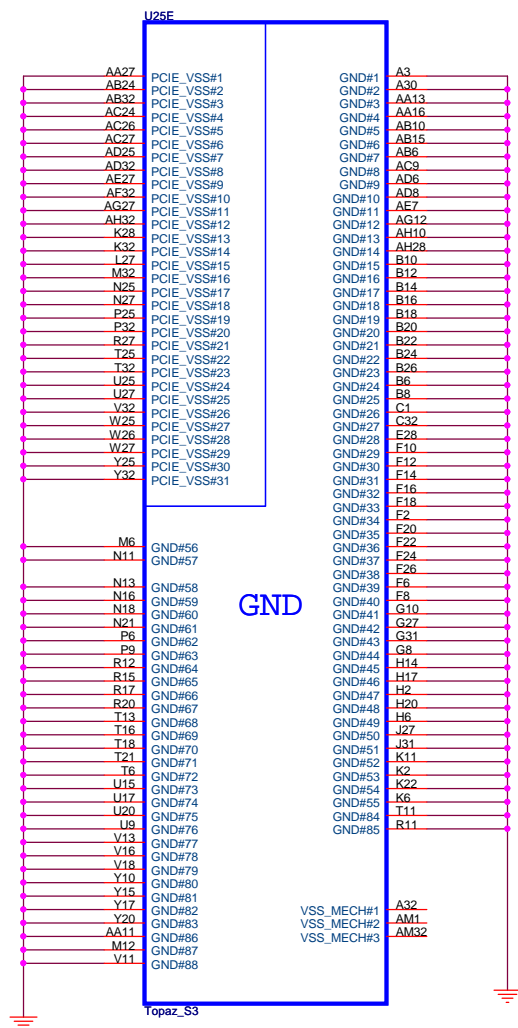


PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Hynix - F(Ruma)	128Mb16 *4, 900MHz	H5TC2G63FMR-11C	NC	4.75K
001	Micron- E die	128Mb16 *4, 900MHz	MT41J128M1GJ7-0930G:R	8.45K	2K
010	Samsung- Q die	128Mb16 *4, 900MHz	K4W3G1646Q-BC1A	4.53K	2K
011	Hynix- Ruma die	256Mb16 *4, 900MHz	H5TC4G63AFR-11C	6.98K	4.99K
100	Samsung- D die	256Mb16 *4, 900MHz	K4W4G1646D-BC1A	4.53K	4.99K
101	Micron- E	256Mb16 *4, 900MHz	MT41J256M16A-0930G:R	3.24K	5.62K

BIT5 => BIT0	
PS0	=> 11001
PS1	=> 11000
PS2	=> 11000
PS3	=> 11000







### CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

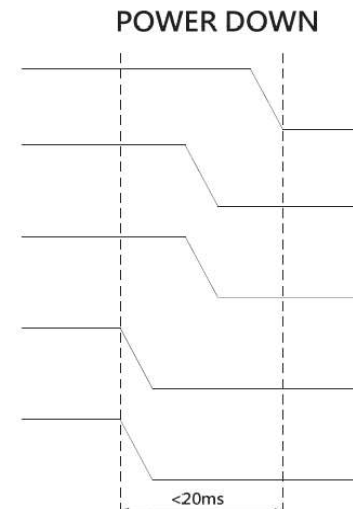
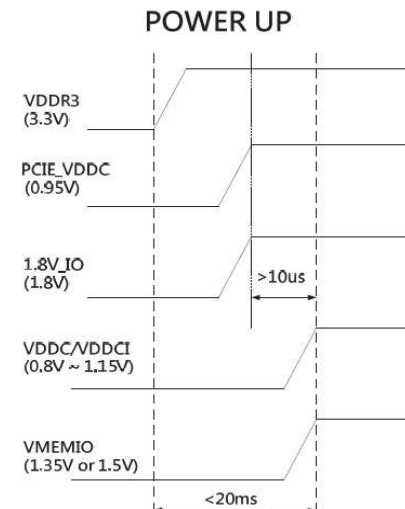
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

### NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED,  
THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

### POWER UP / POWER DOWN SEQUENCE

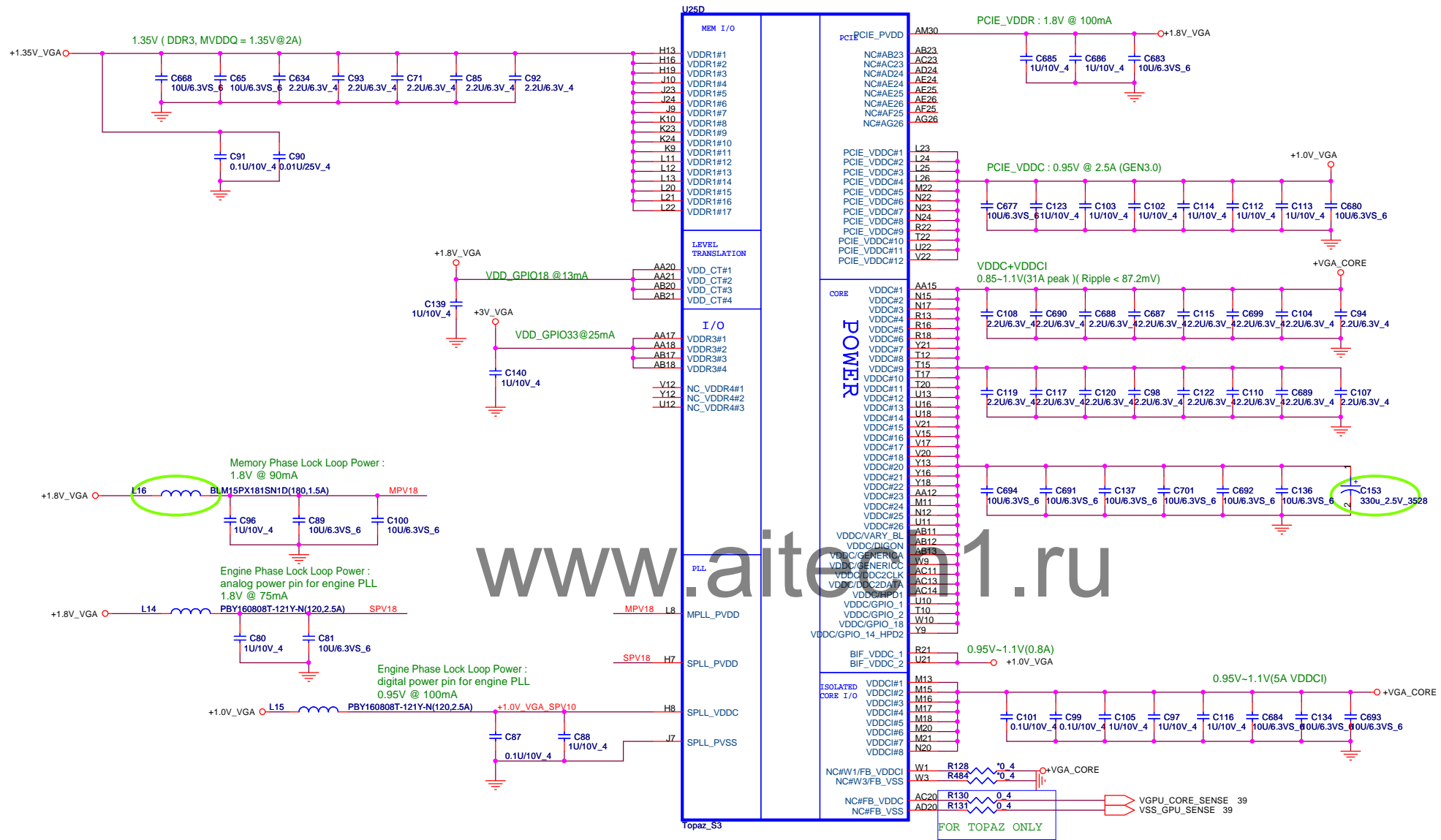


**PROJECT : Y21A**  
Quanta Computer Inc.  
KAVERI

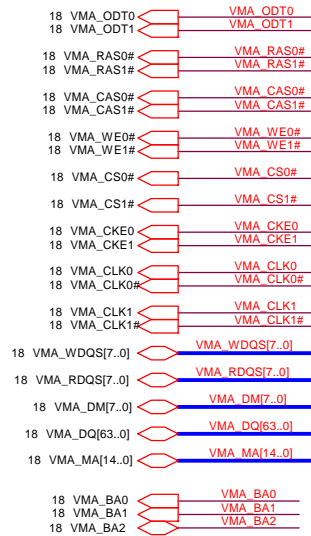
Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A

Thursday, February 06, 2014

Sheet 41



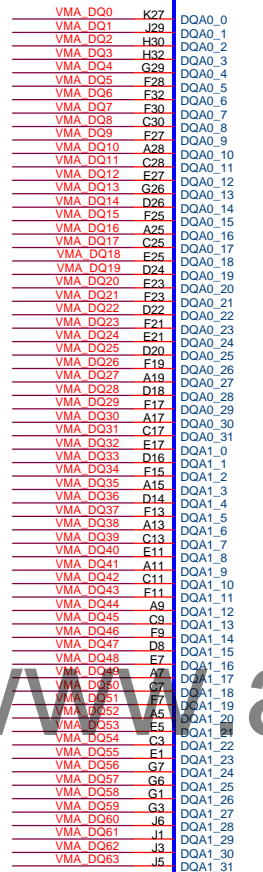
+1.35V\_VGA 17,18,39  
+1.8V\_VGA 13,14,29,39,41  
+1.0V\_VGA 13,41  
+VGA\_CORE 39,40

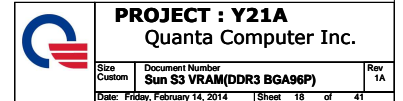


support 1Gbit  
VRAM ( 64M X 16 )

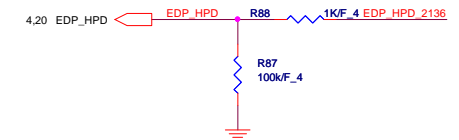
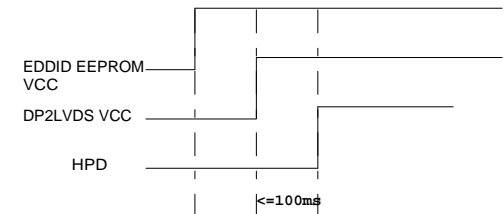
U25C

## MEMORY INTERFACE

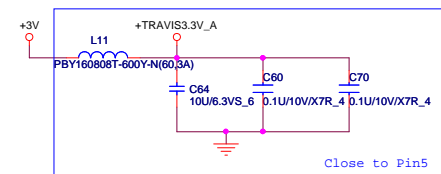
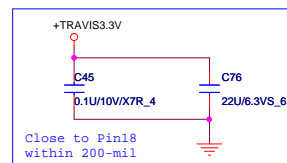
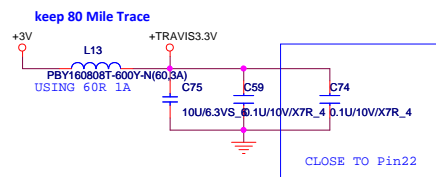
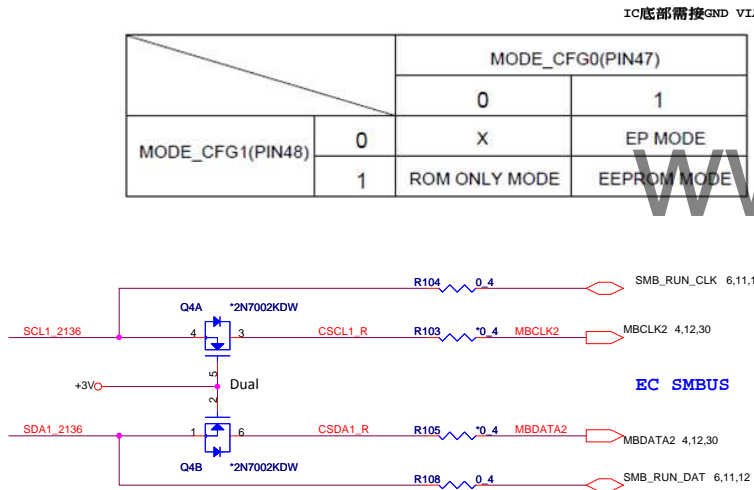
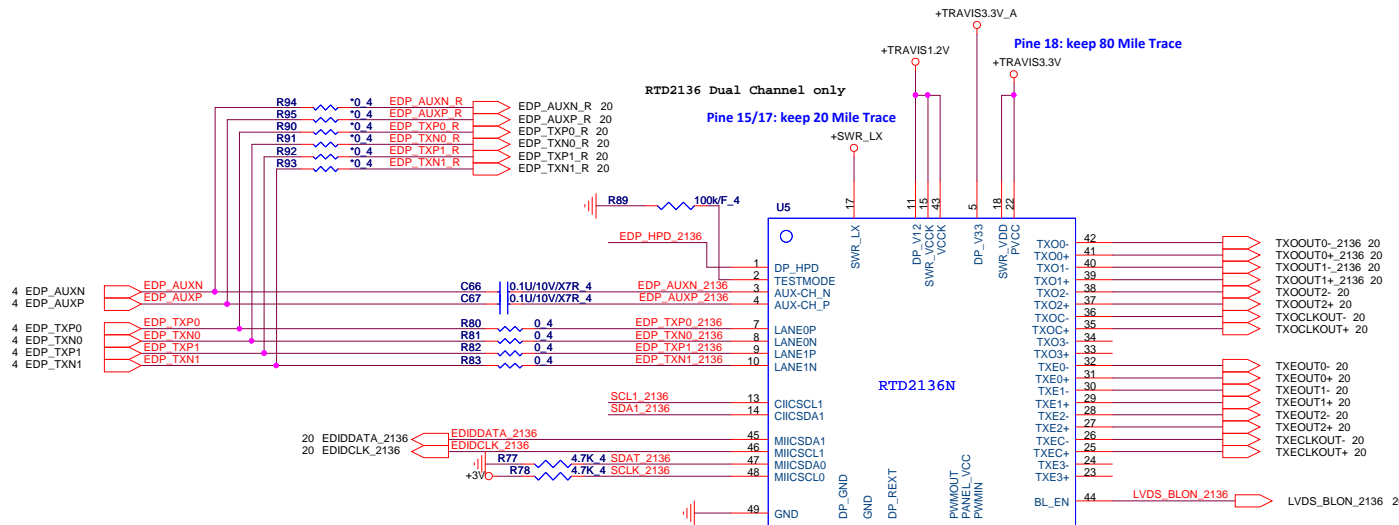
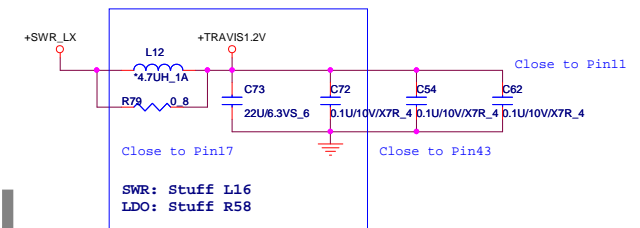




## RTD2136S Power Up Sequence



L69: need use CV-4709MN00 for Vendor suggestion  
2nd CV-4708MN03



2,4,6,8,9,10,11,12,20,21,22,23,24,25,26,27,28,29,30,38 +1.35V  
+3V  
2,4,22,27,29,34 +1.5V



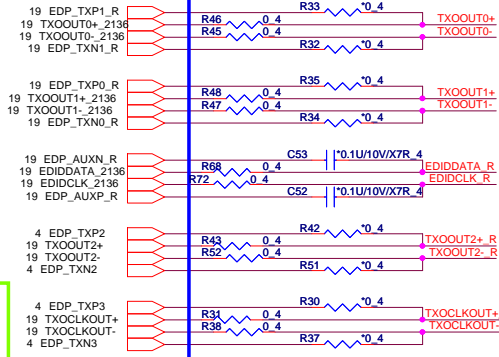
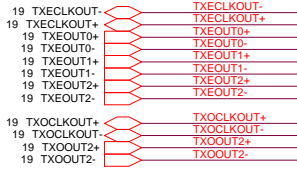
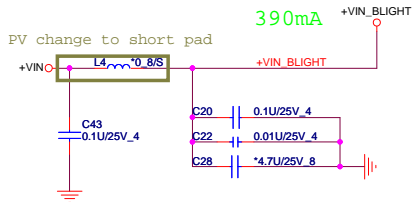
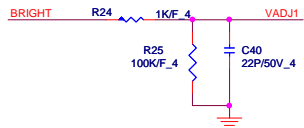
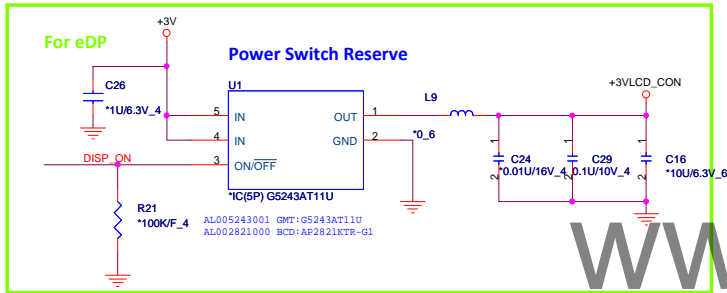
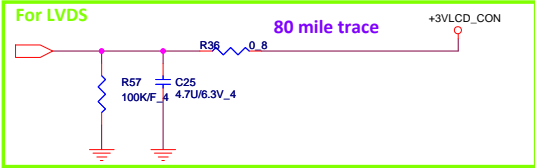
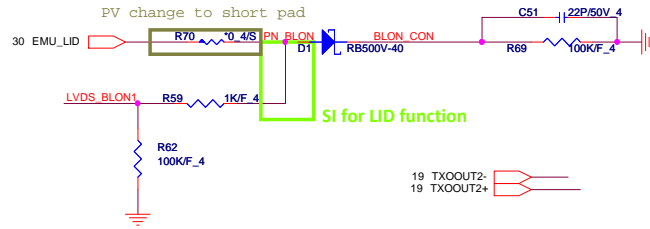
**PROJECT : Y21A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	LVDS converter RTD2136	1A
Date: Friday, February 14, 2014	Sheet 19 of 41	



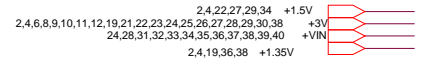
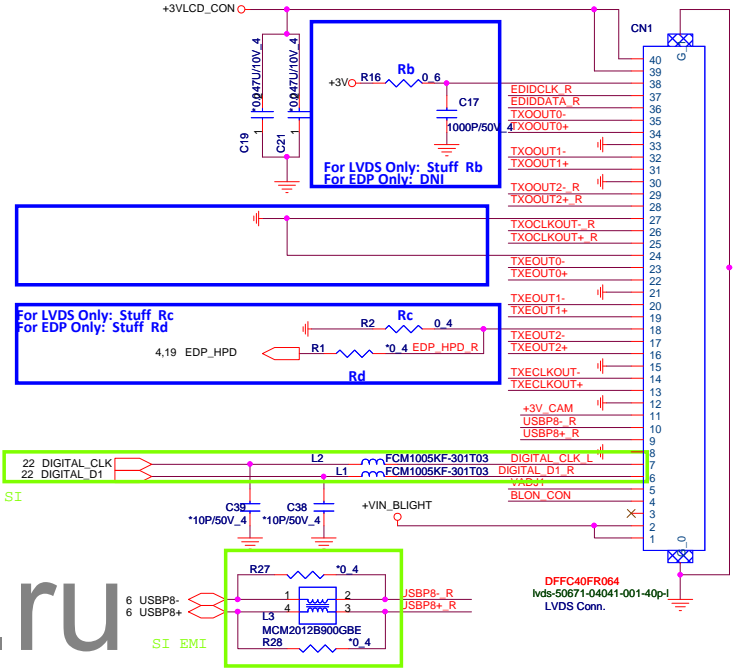
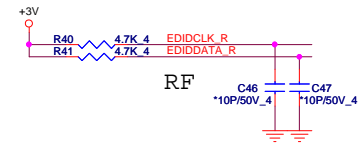
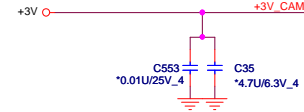
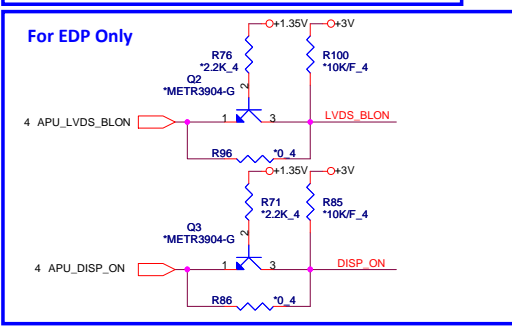
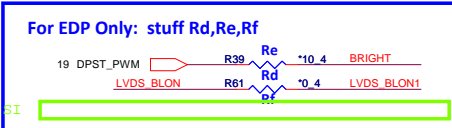
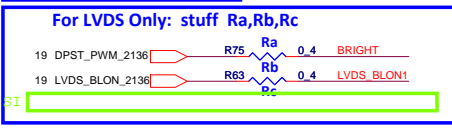
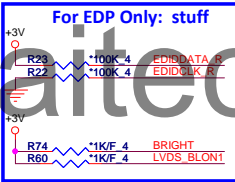
# LVDS conn.

20



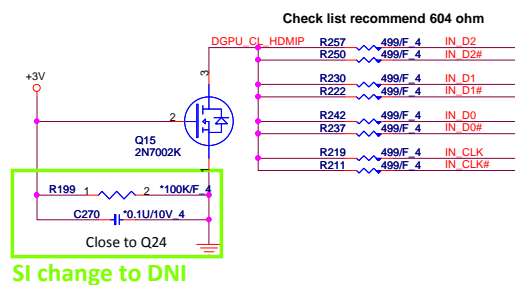
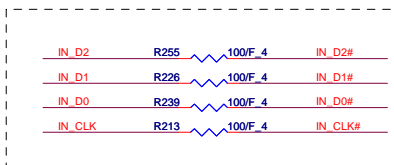
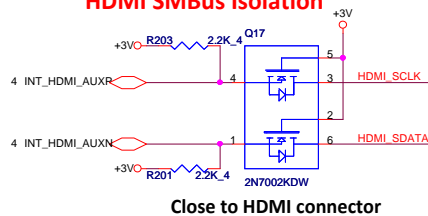
For EDP Only: stuff  
R37/R45/R72/R72/R74/R77/R82/R79/R118/R89

For LVDS only: stuff  
R17/R18/R11/R120/R33/R34/R56/R81/R90/R109

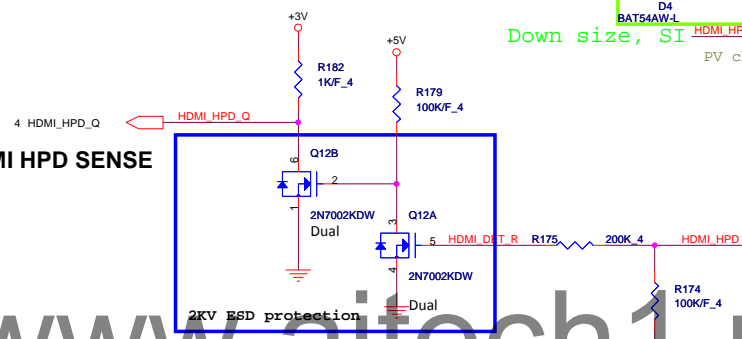


## HDMI Conn.

## HDMI SMBus Isolation



## HDMI HPD SENSE

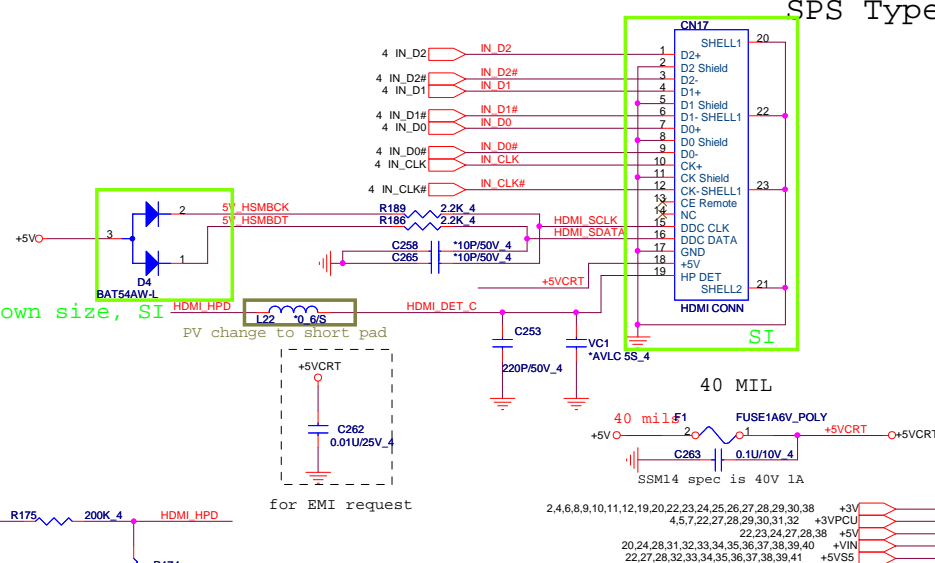


Down size, SI

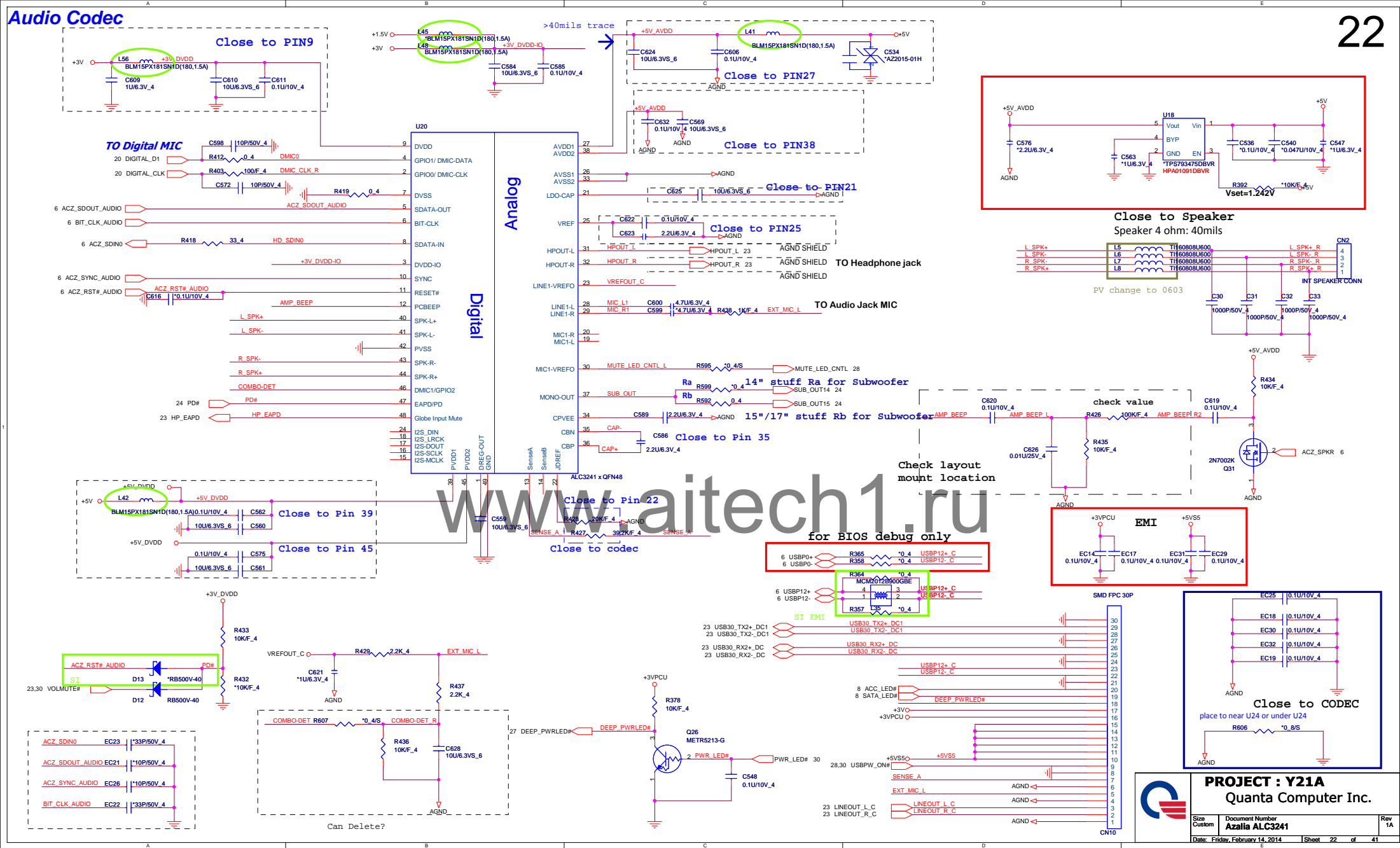
PV change to short pad

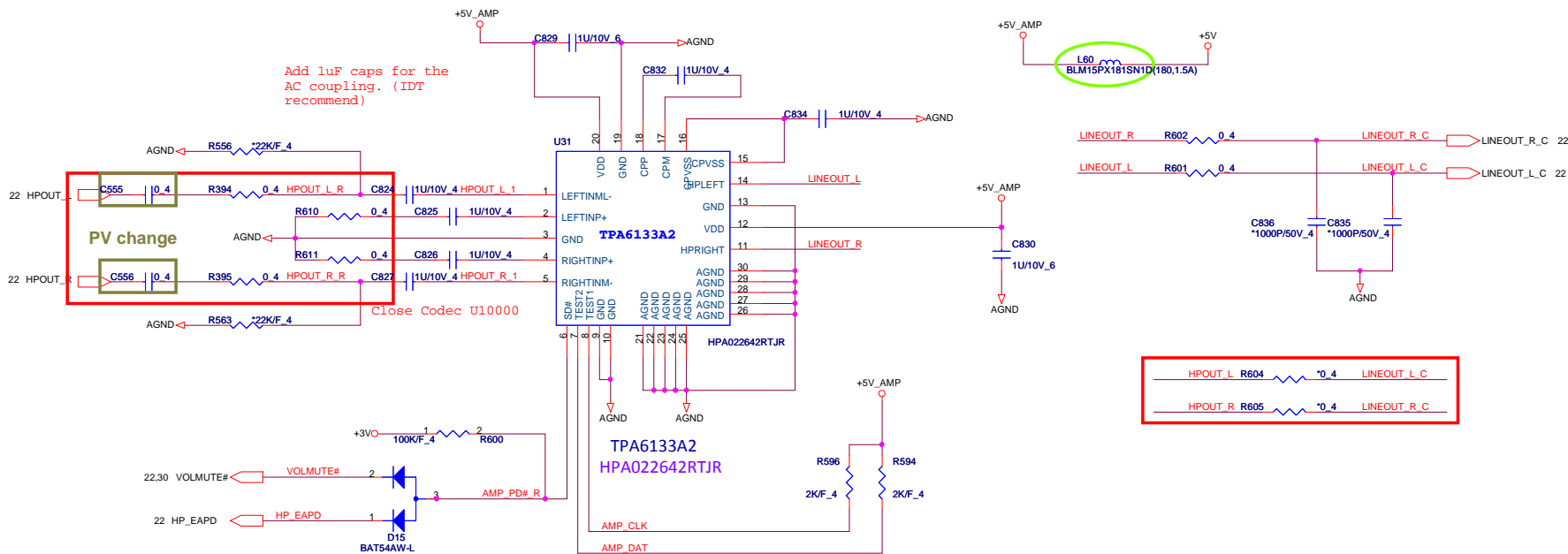
for EMI request

## SPS Type



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## USB3.0 re-driver

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From HOST

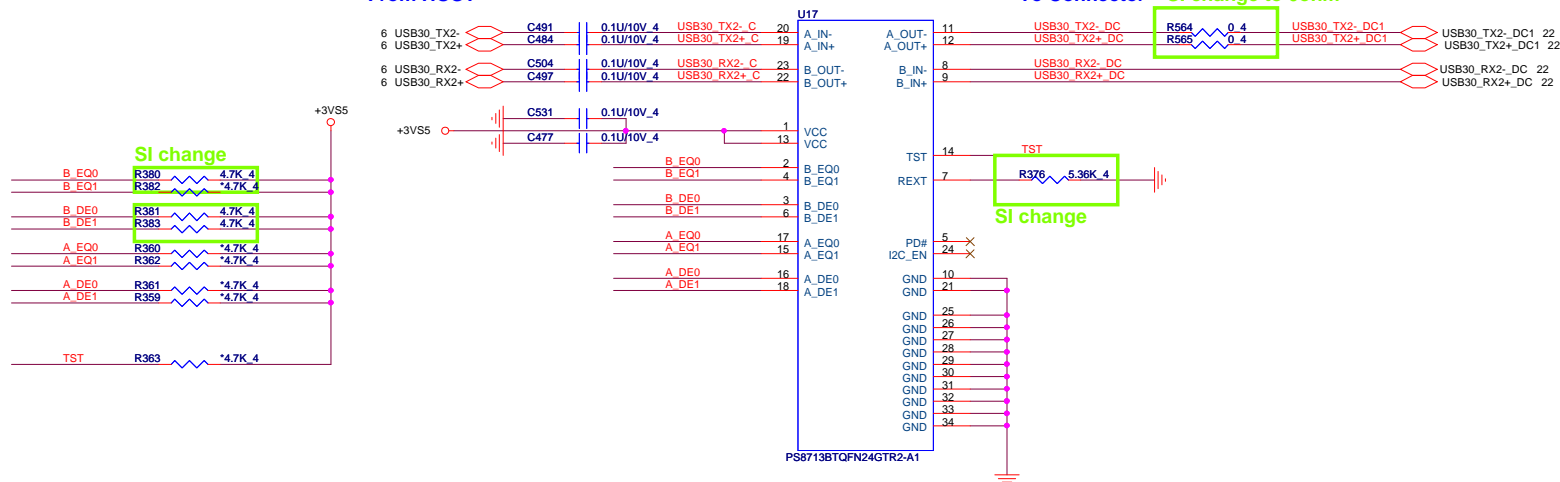
USB3.0 Re-driver

To Connector

SI change to 0ohm

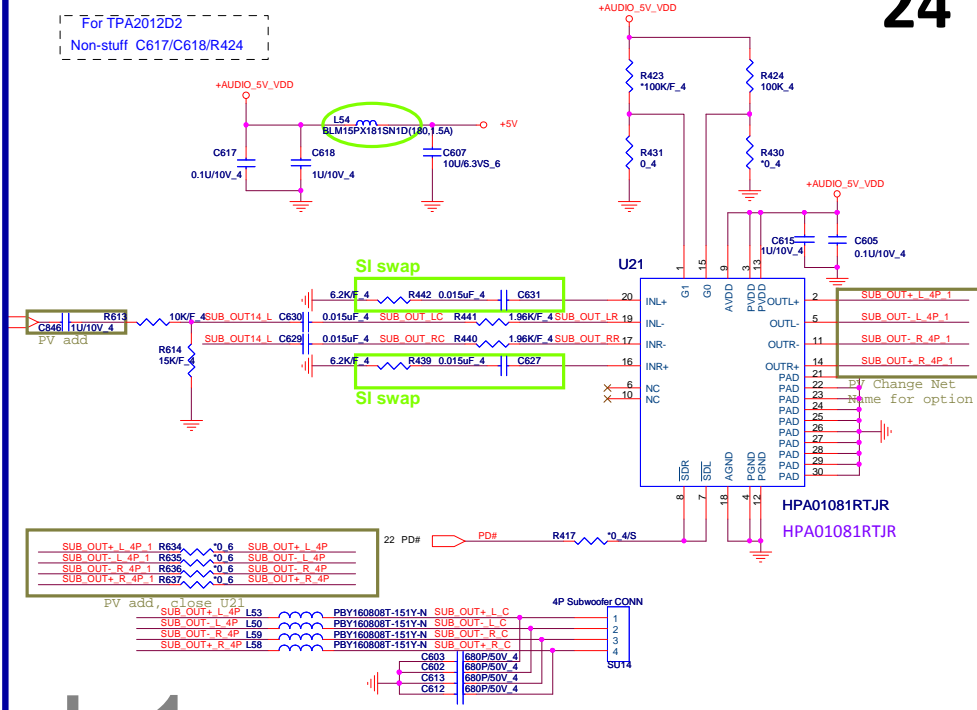
A_EQ0	A_EQ1		A_DE0	A_DE1	
B_EQ0	B_EQ1		B_DE0	B_DE1	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

TST : Low = Normal LFPS swing / High =Turn down LFPS swing

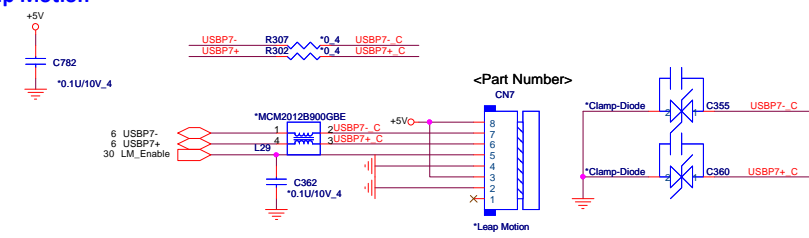
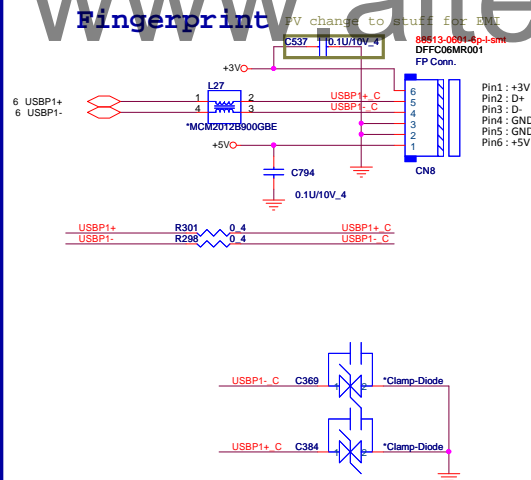



24

For TPA2012D2  
Non-stuff C617/C618/R424

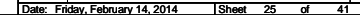


## Leap Motion



	<b>PROJECT : Y21A</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>Subwoofer/FP/Leap Motion</b>	Rev 1A
	Date: Friday, February 21, 2014	Sheet 24 of 41	





6 CLK\_PCIE\_REQ2# R547 0.4S CLK\_PCIE\_REQ2# R

PV change to short pad

7 CARD\_PCIE\_RST# R548 0.4 CLK\_PCIE\_REQ2# R

Zdiff = 100 ohm

2 PCIE\_TXP2\_CARD  
2 PCIE\_TXN2\_CARD  
7 CLK\_PCIE\_CARDP  
7 CLK\_PCIE\_CARDN  
2 PCIE\_RXP2\_CARD  
2 PCIE\_RXN2\_CARD

C779 0.1U/10V\_4 PCIE\_RXP2\_CARD C  
 C780 0.1U/10V\_4 PCIE\_RXN2\_CARD C

Please add 9 GND VIAS  
connection with thermal PAD

R357 need close to Chip

C792 10U/6.3VS\_6  
 C790 0.1U/10V\_4

CLOSE CONN

C558 0.1U/10V\_4  
 C556 0.1U/10V\_4  
 C581 10U/6.3V\_6

CARD READER  
CN11

SD D3 1 DAT3  
 SD CMD 2 CMD  
 3 VSS1  
 4 VDD  
 5 CLK  
 6 VSS2  
 7 DAT0  
 8 DAT1  
 9 DAT2  
 10 W/P  
 11 C/D  
 12 GND  
 13 GND  
 14 GND  
 15 GND

Change footprint to  
sdcard-psdbtc-09glbs1nn4h3-11p

Close to chip pin

Close to chip pin

PV, EMI suggestion

Share Pin

SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Reserve for EMI

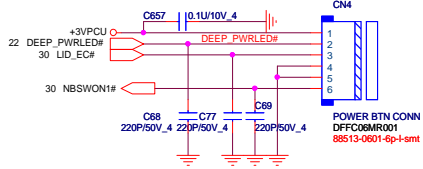
SD D0 EC16 5.6P/16V\_4  
 SD D1 EC15 5.6P/16V\_4  
 SD D2 EC24 5.6P/16V\_4  
 SD D3 EC20 5.6P/16V\_4



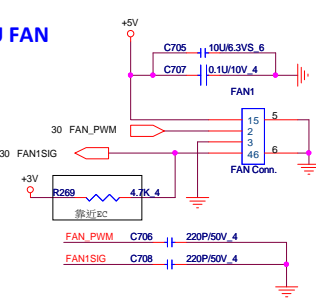
**PROJECT : Y21A**  
Quanta Computer Inc.

Size Custom	Document Number <b>RTS5239 &amp; CR SOCKET</b>	Rev 1A
Date: Friday, February 14, 2014	Sheet 26 of 41	

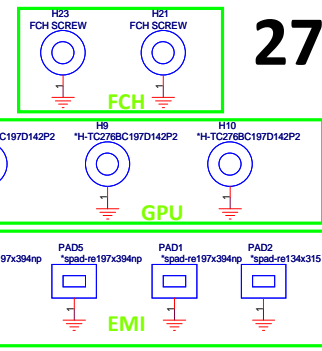
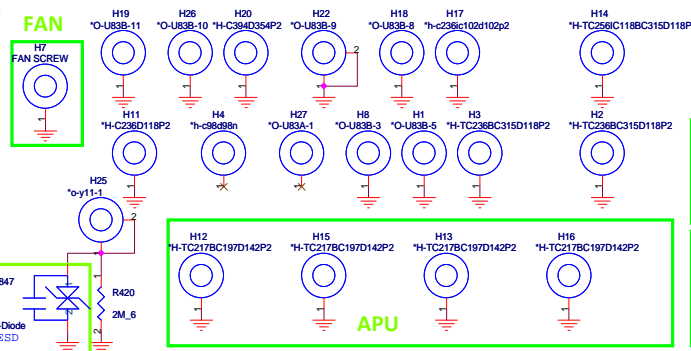
## Power Button Connector



## CPU FAN

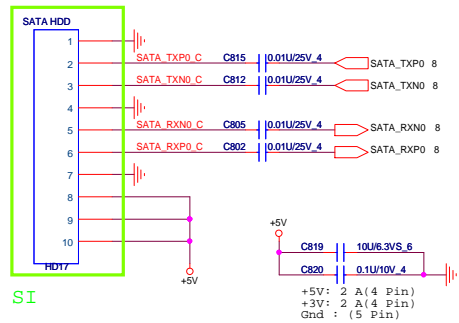


## Hole FAN

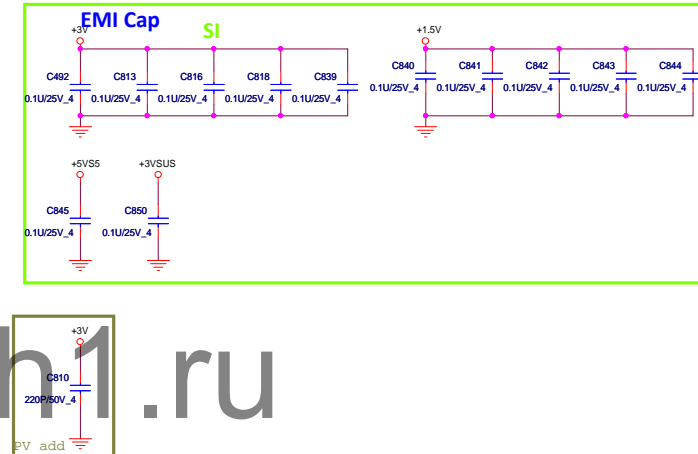
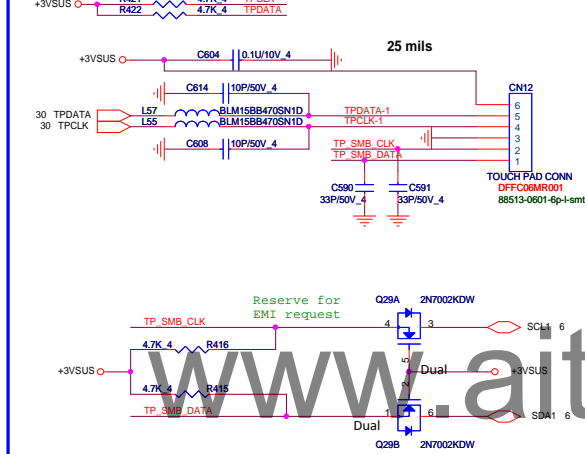


27

## SATA HDD Connector(Cable type)

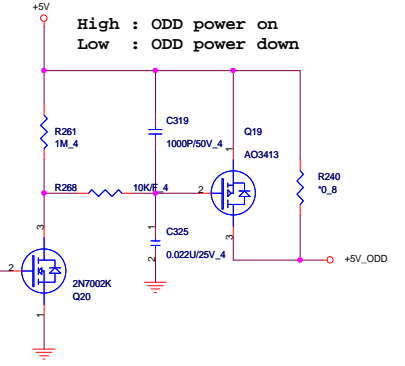
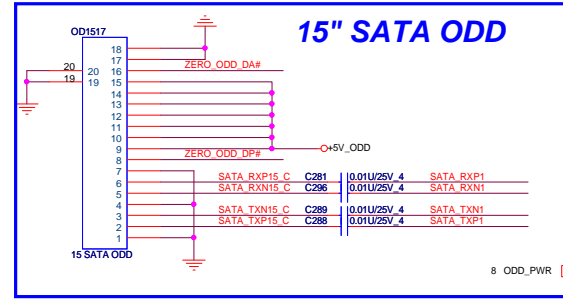
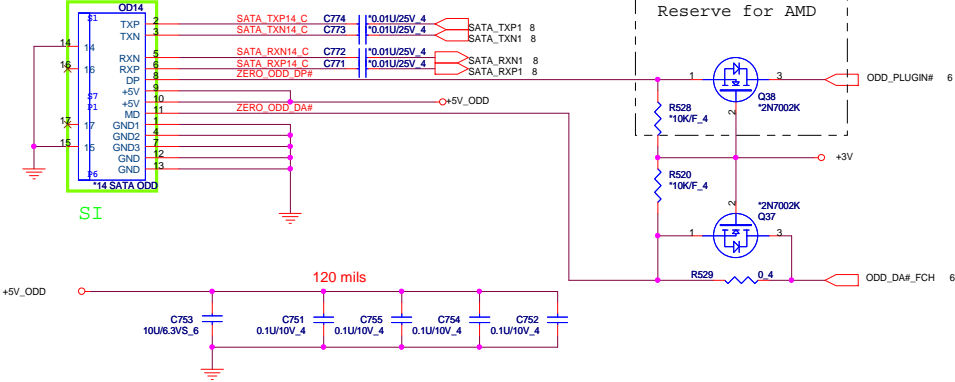


## Touch Pad

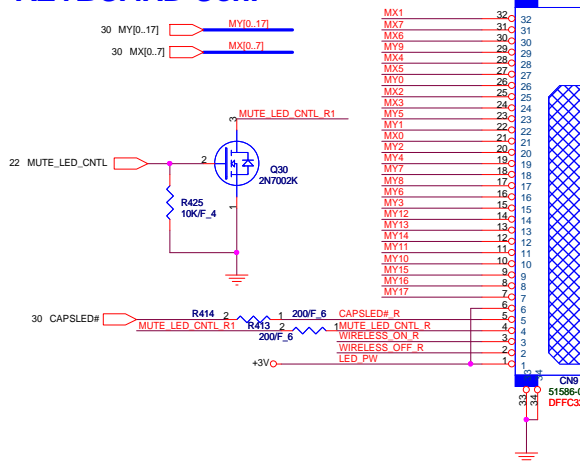


## SATA ODD CONNECTOR

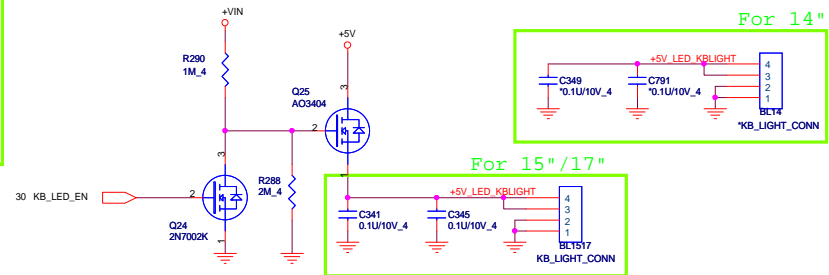
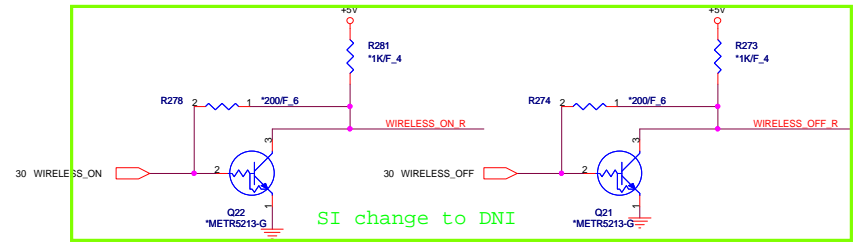
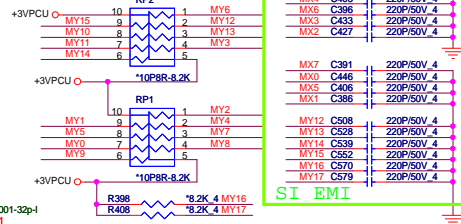
### NEW Type Bypass CAP close conn



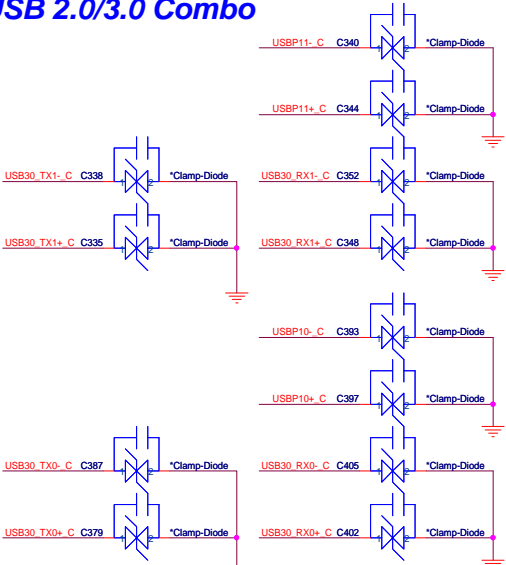
## KEYBOARD Con.

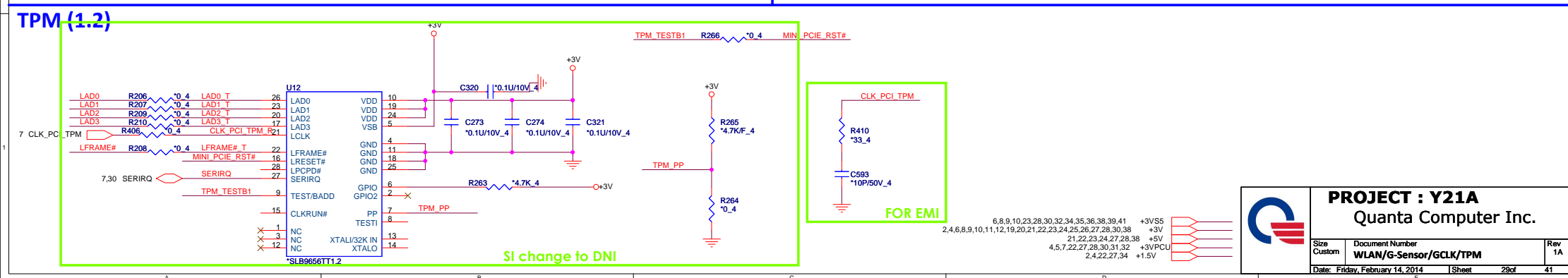
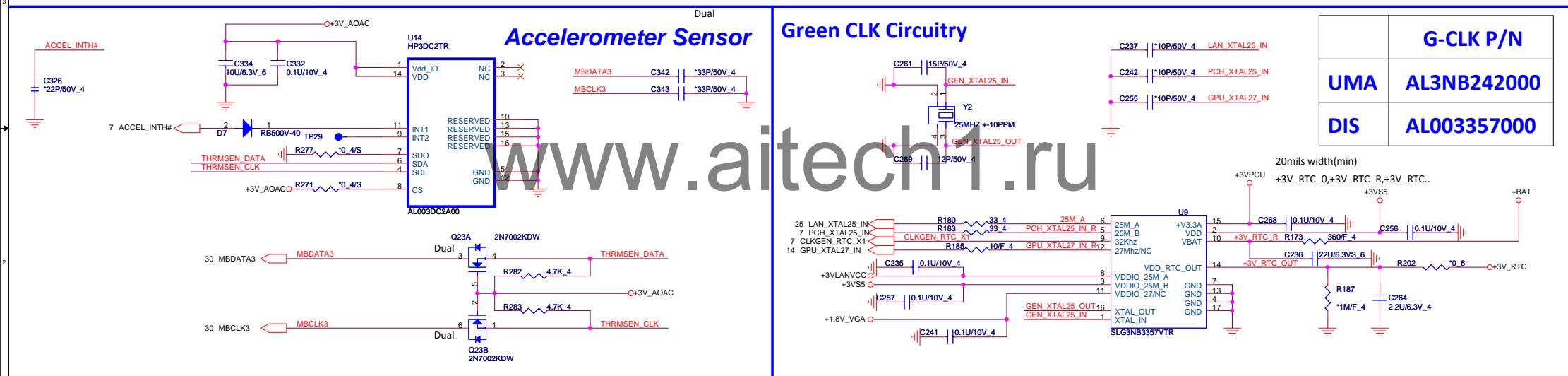
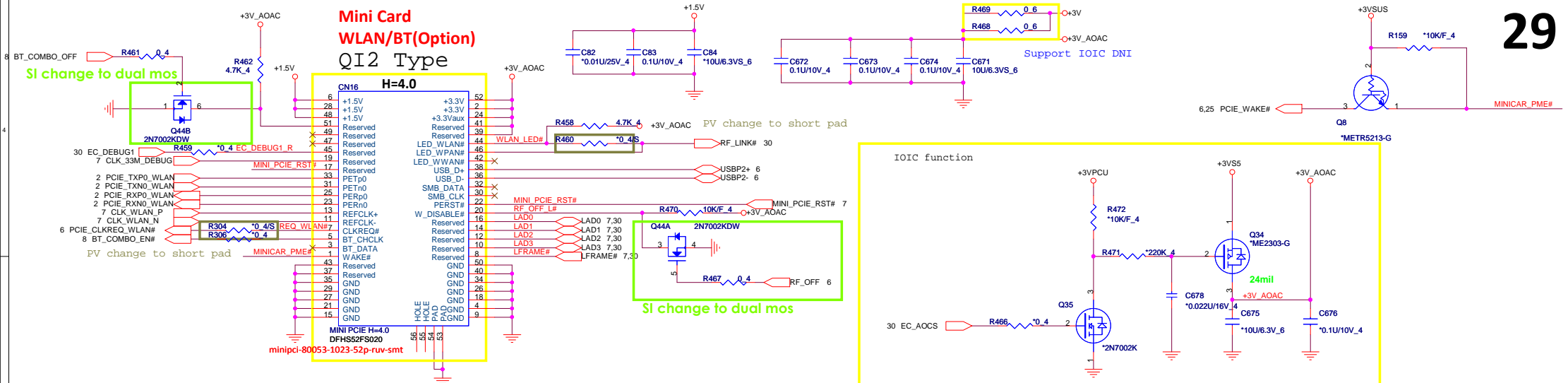


## KEYBOARD PULL-UP



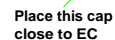
## USB 2.0/3.0 Combo

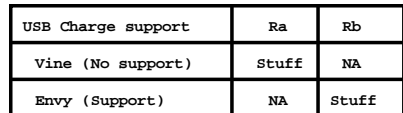
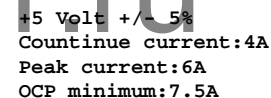
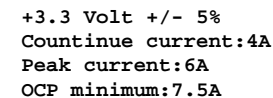










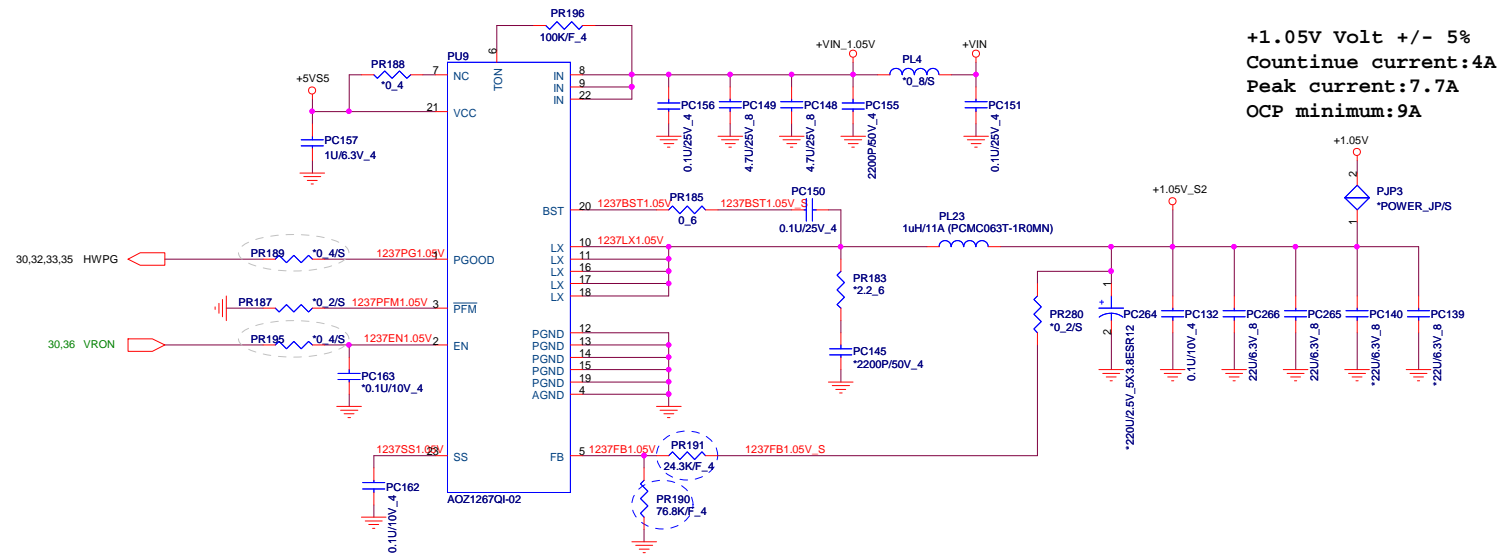




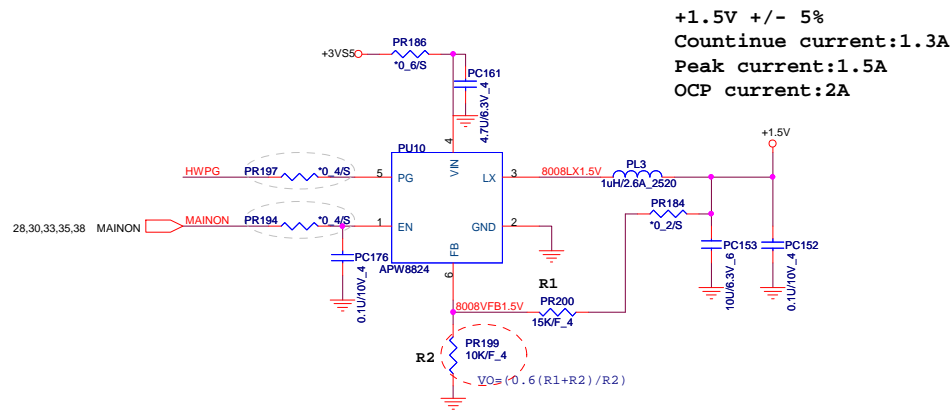
 +1.35VSUS 2,3,4,5,11,12,38



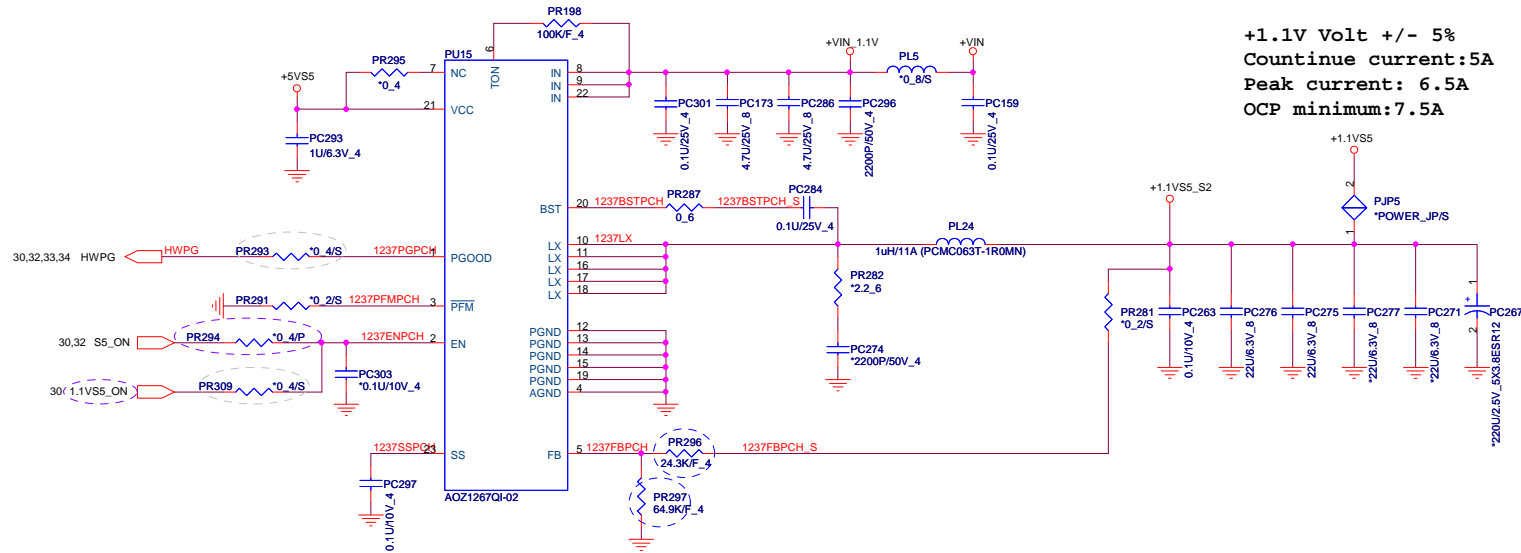
Date: Friday, February 14, 2014	Sheet 33 of 41
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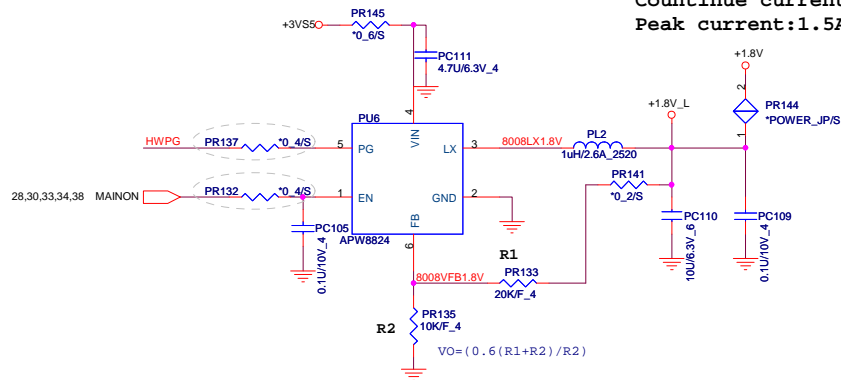


+VIN 20,24,28,31,32,33,35,36,37,38,39,40  
+3VS5 6,8,9,10,23,28,29,30,32,35,36,38,39,41  
+5VS5 22,27,28,32,33,35,36,37,38,39,41  
+5VPCU 31,32



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**+1.8V +/- 5%**  
**Countinue current:0.8A**  
**Peak current:1.5A**

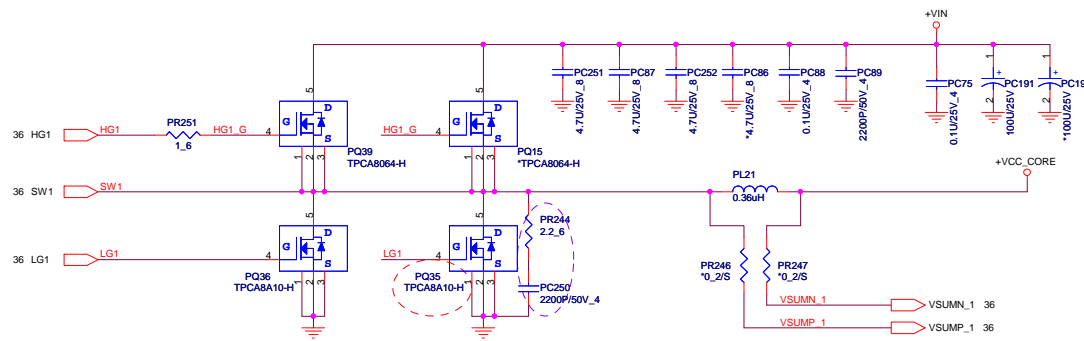


+VIN 20,24,28,31,32,33,34,36,37,38,39,40  
+3VS5 6,8,9,10,23,28,29,30,32,34,36,38,39,41  
+5VS5 22,27,28,32,33,34,36,37,38,39,41  
+1.1VS5 9,38  
+5VPCU 31,32

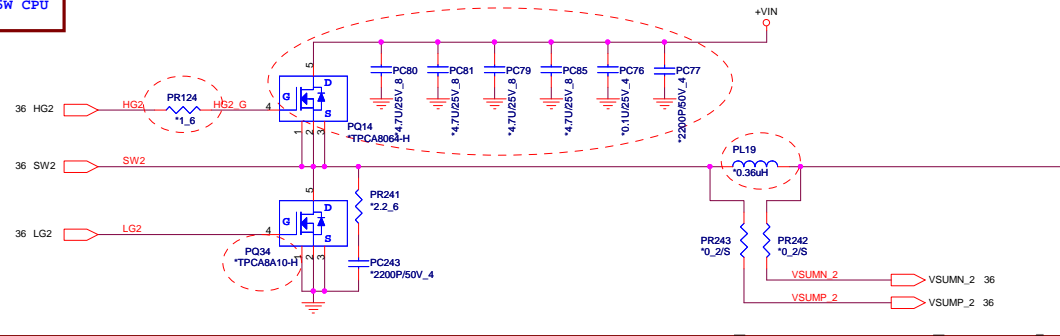




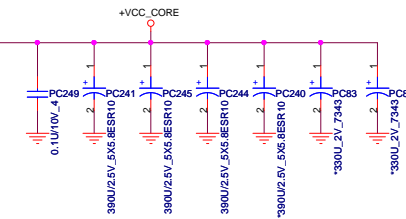
CPU TYPE	MOSFET
19W	1H2L/1phase



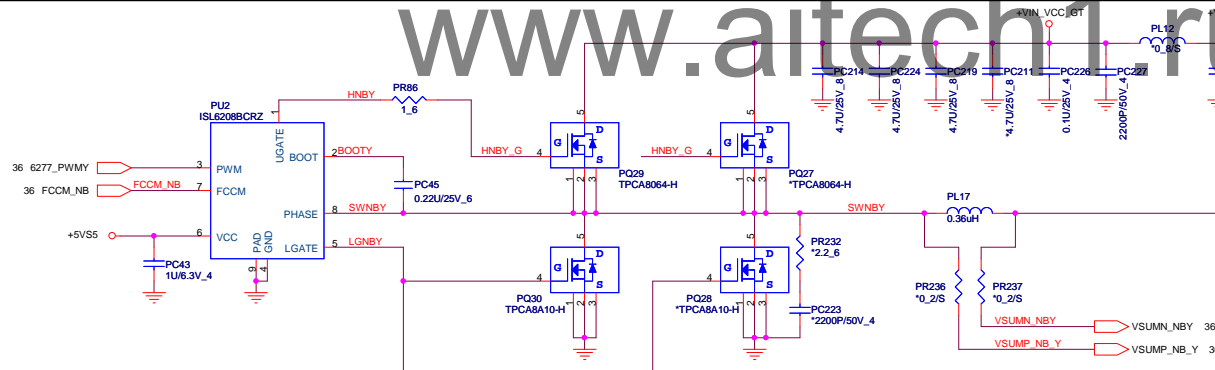
Only for 25W CPU



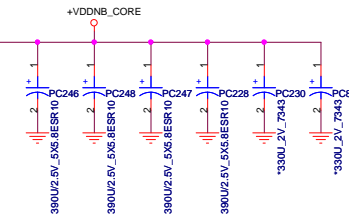
CPU CORE Volt (19W)  
Continue current: 22A  
Peak current: 38A  
OCP minimum: 45A



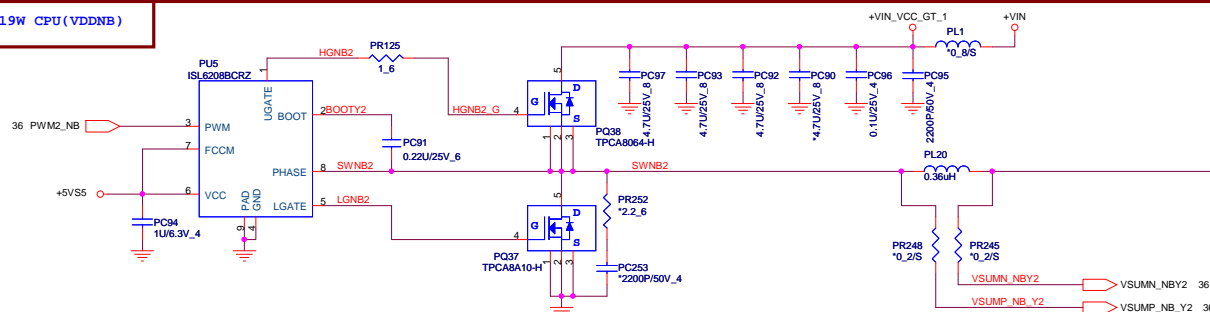
CPU TYPE	MOSFET
19W	1H1L/2phase

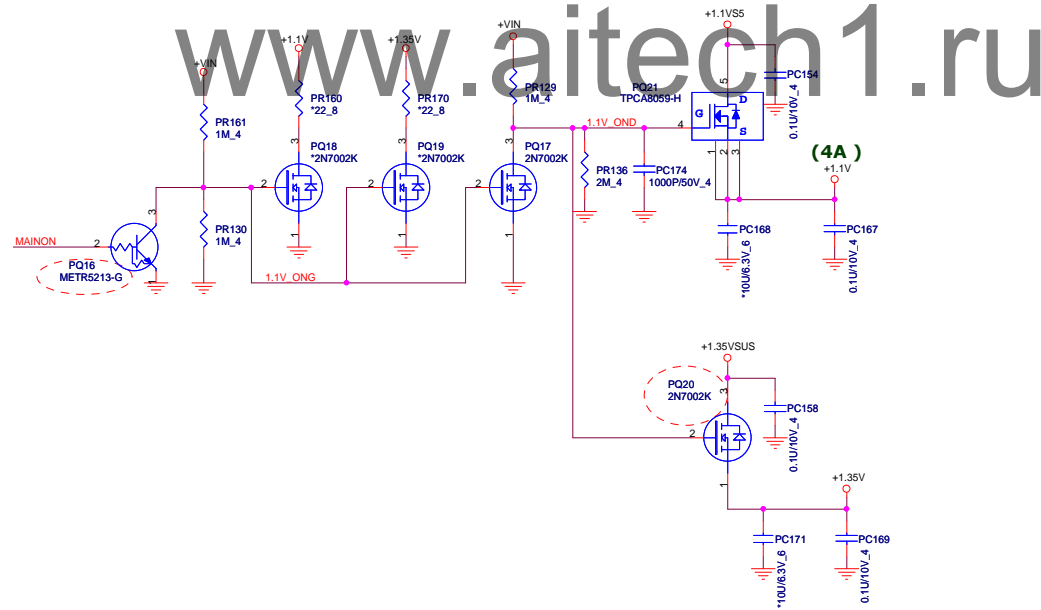
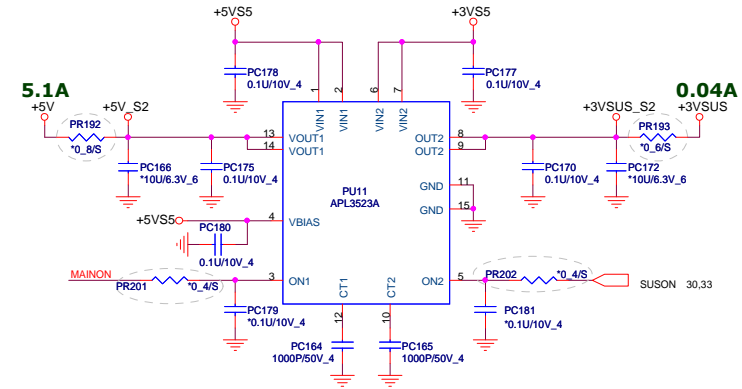
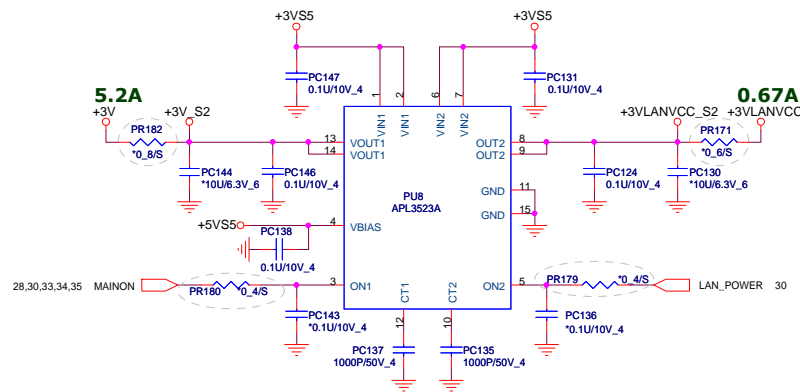


VDDNB Volt  
Continue current: 28A  
Peak current: 40A  
OCP minimum: 47A



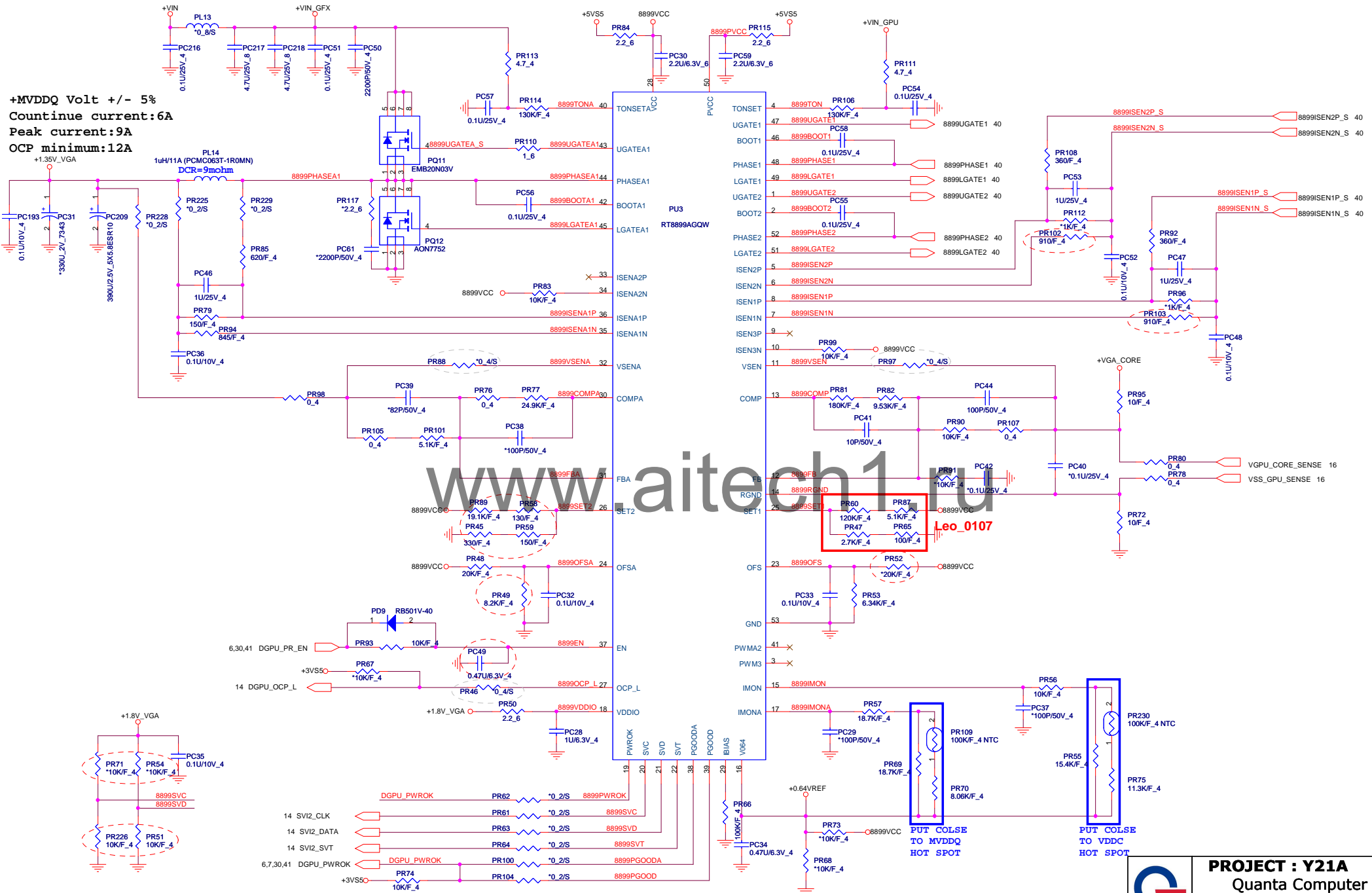
19W CPU (VDDNB)





2,4,6,8,9,10,11,12,19,20,21,22,23,24,25,26,27,28,29,30	+3V
21,22,23,24,27,28	+5V
20,24,28,31,32,33,34,35,36,37,39,40	+VIN
6,8,9,10,23,28,29,30,32,34,35,36,39,41	+3VS5
22,27,28,32,33,34,35,36,37,39,41	+5VS5
25,29	+3VLAVCC

+MVDDQ Volt +/- 5%  
 Countinue current:6A  
 Peak current:9A  
 OCP minimum:12A



**PROJECT : Y21A**  
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	Vcore( RT8899A)	1A
Date: Friday, February 14, 2014	Sheet 39 of 41	

